

Compal Confidential

PBL60 Schematics Document

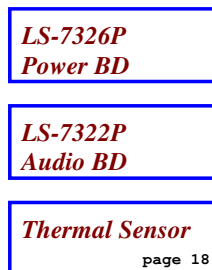
AMD APU Zacate-FT1 + FCH Hudson-M1 + GPU Seymour XT-M2

www.aitech1.ru

2010-02-15

REV: 1.0

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				P02-Block Diagrams				
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SMBUS Control Table

	SOURCE	MIINI1	BATT	APU	FCH	SODIMM	VRAM
EC_SMB_CK1 EC_SMB_DAI1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DAI2	KB930	X	X	V	V	X	V
FCH_SMCLK0 FCH_SMDAT0	FCH (+3VS)	V	X	X	X	V	X
FCH_SMCLK3 FCH_SMDAT3	FCH (+3VALW)	X	X	V	X	X	X

BOM Structure

15G@: 1.5G CPU (E240)
16G@: 1.6G CPU (E350)
1G@ : 1G CPU (C50)
UMA@ : APU output.
VGA@ : GPU used.
LS@ : Level shift used.
X76@L01 :VRAM 1G.
X76@L03 :VRAM 512M.

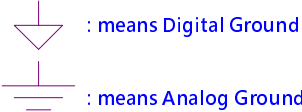
FCH Hudson-M1 USB Port List	
USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	JUSB1
Port1	JUSB2
Port2	Camera
Port3	JMINI (WLAN)
Port4	Card Reader
Port5	JUSB3
Port6	NC
Port7	NC
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List		
APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M1 SATA Port List	
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

SCL0, SDA0 (Primary SMBUS in the S0 domain)
SCL1, SDA1 (Secondary SMBUS supporting ASF)
SCL2, SDA2 (Primary SMBUS in the S5 domain)
SCL3, SDA3 (Primary low-voltage SBMBUS for Processor TSI)
SCL4, SDA4 (Primary SMBUS in the S5 domain)

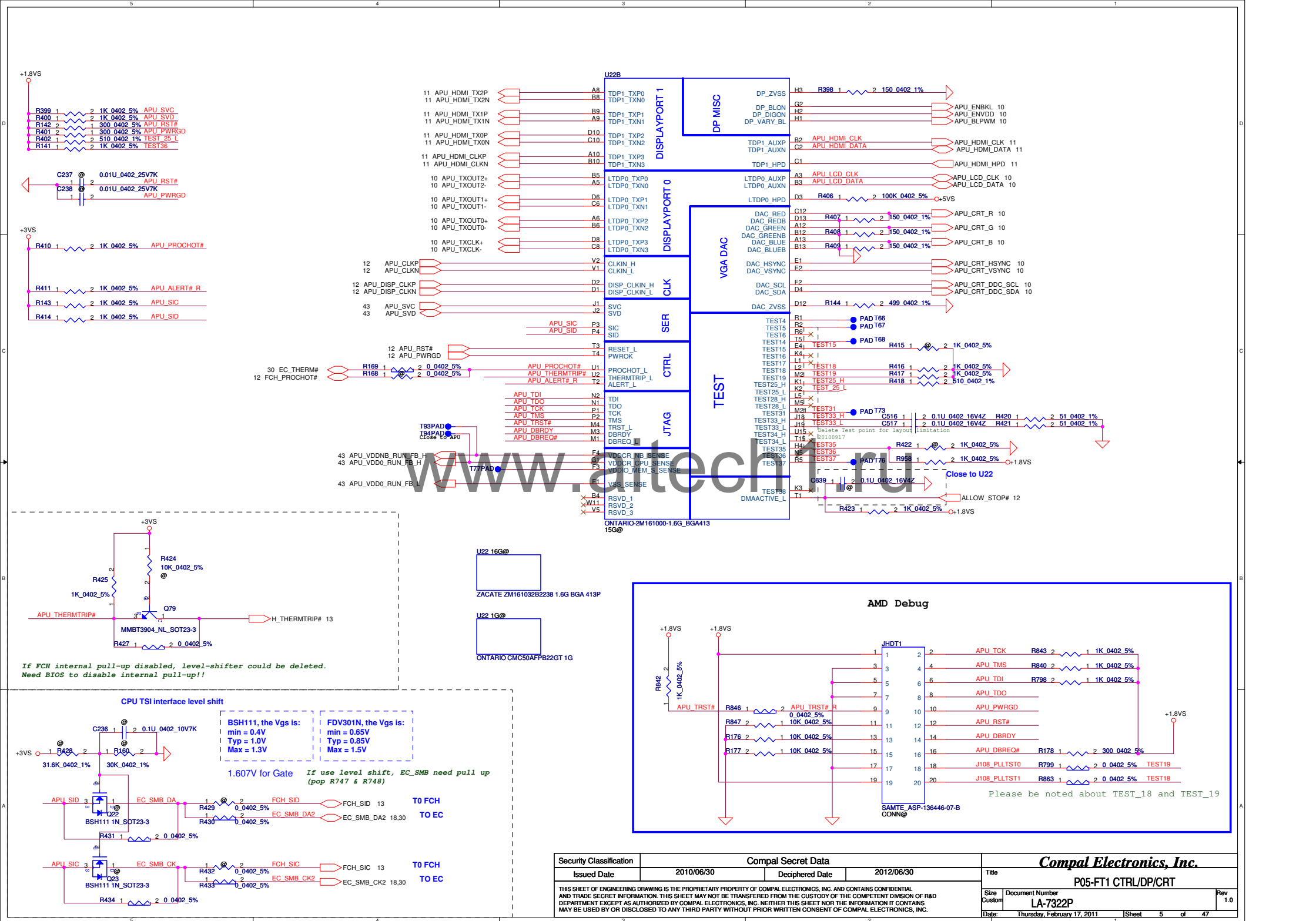
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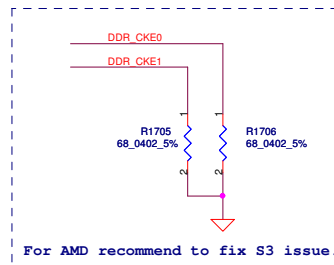
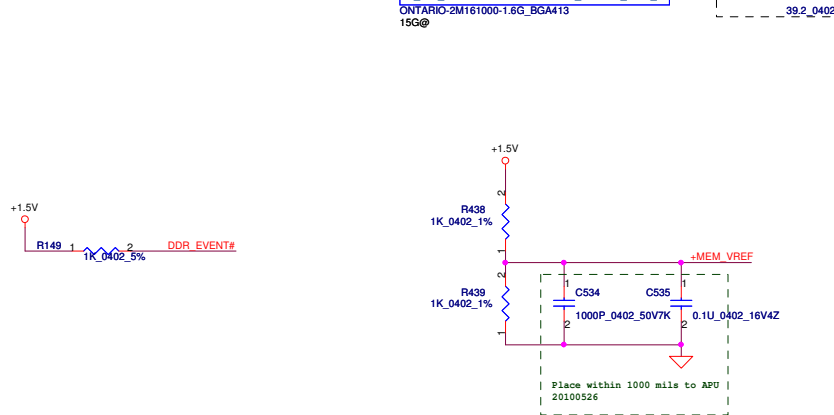
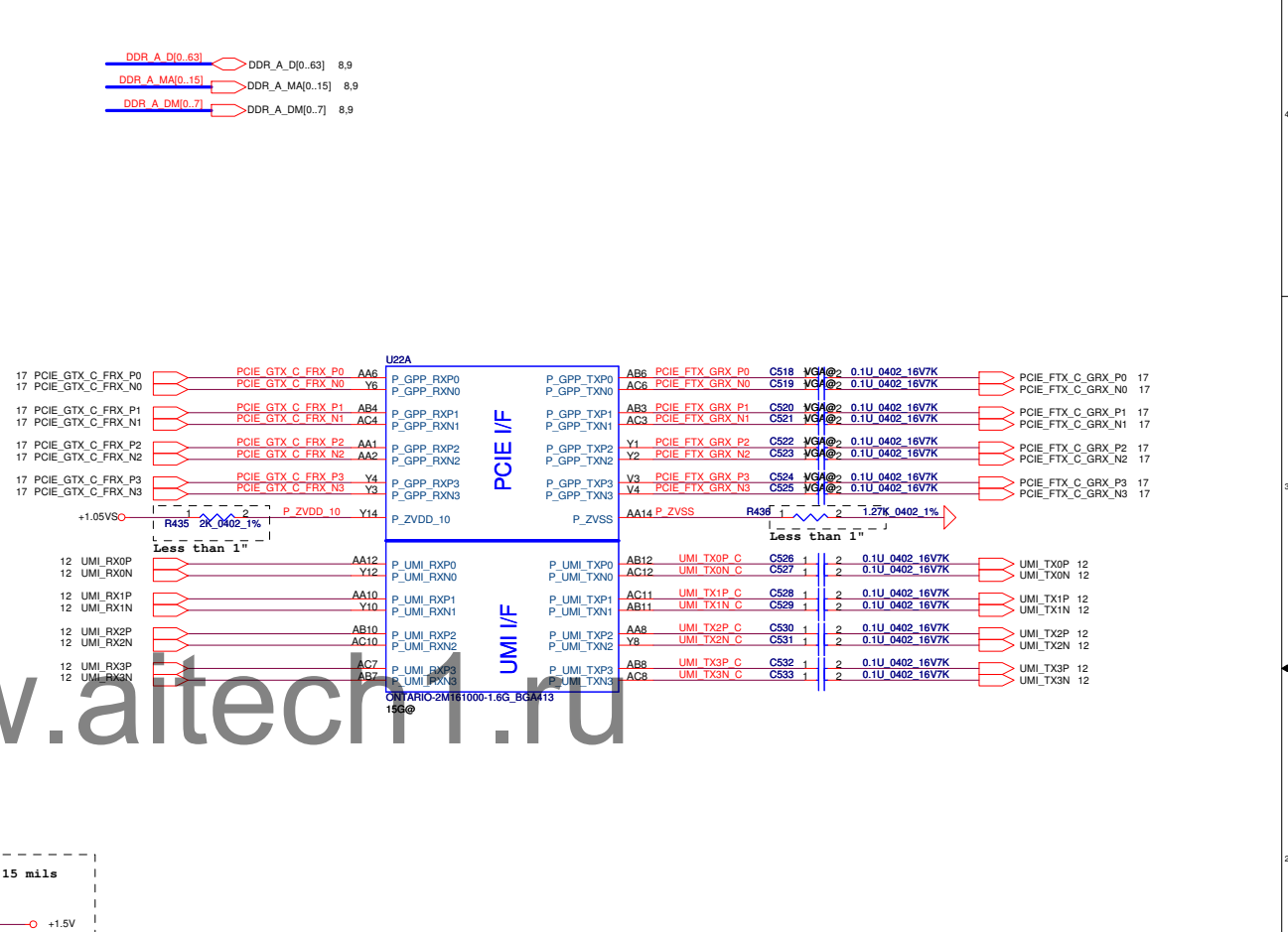
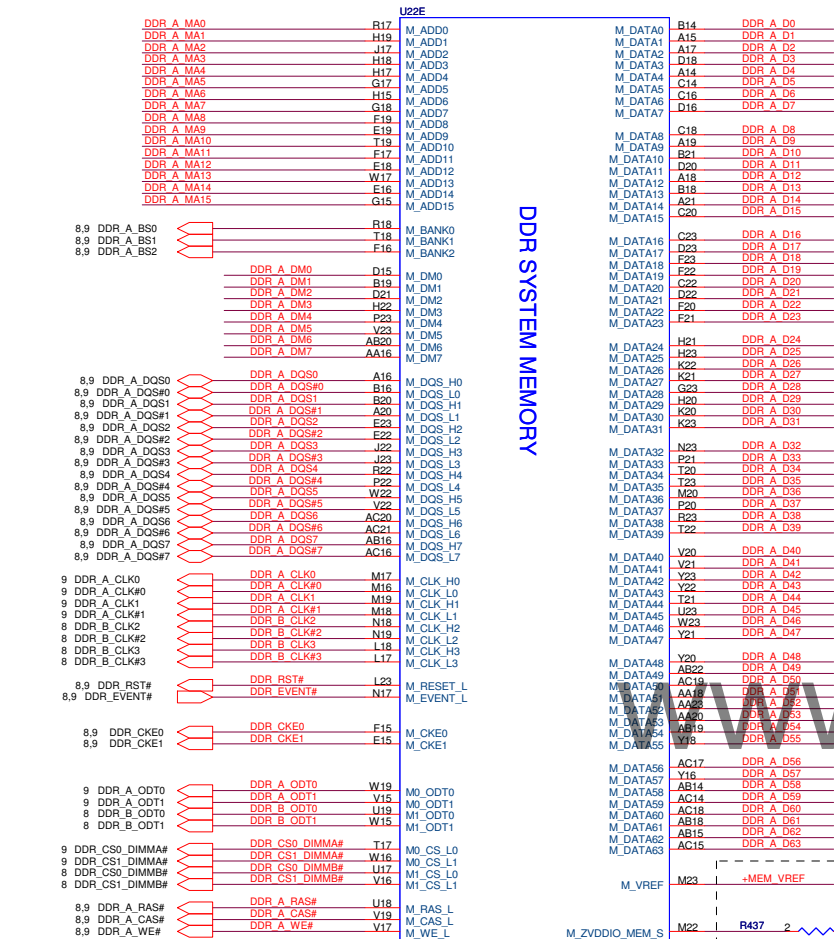


- L01 : 16G@/VGA@/LS@/X76@L03
- L02 : 16G@/UMA@/LS@
- L03 : 15G@/VGA@/LS@/X76@L03
- L04 : 15G@/UMA@/LS@
- L05 : 16G@/VGA@/LS@/X76@L01
- L06 : 15G@/VGA@/LS@/X76@L01
- L07 : 1G@/VGA@/LS@/X76@L03
- L08 : 1G@/UMA@/LS@
- L09 : 1G@/VGA@/LS@/X76@L01

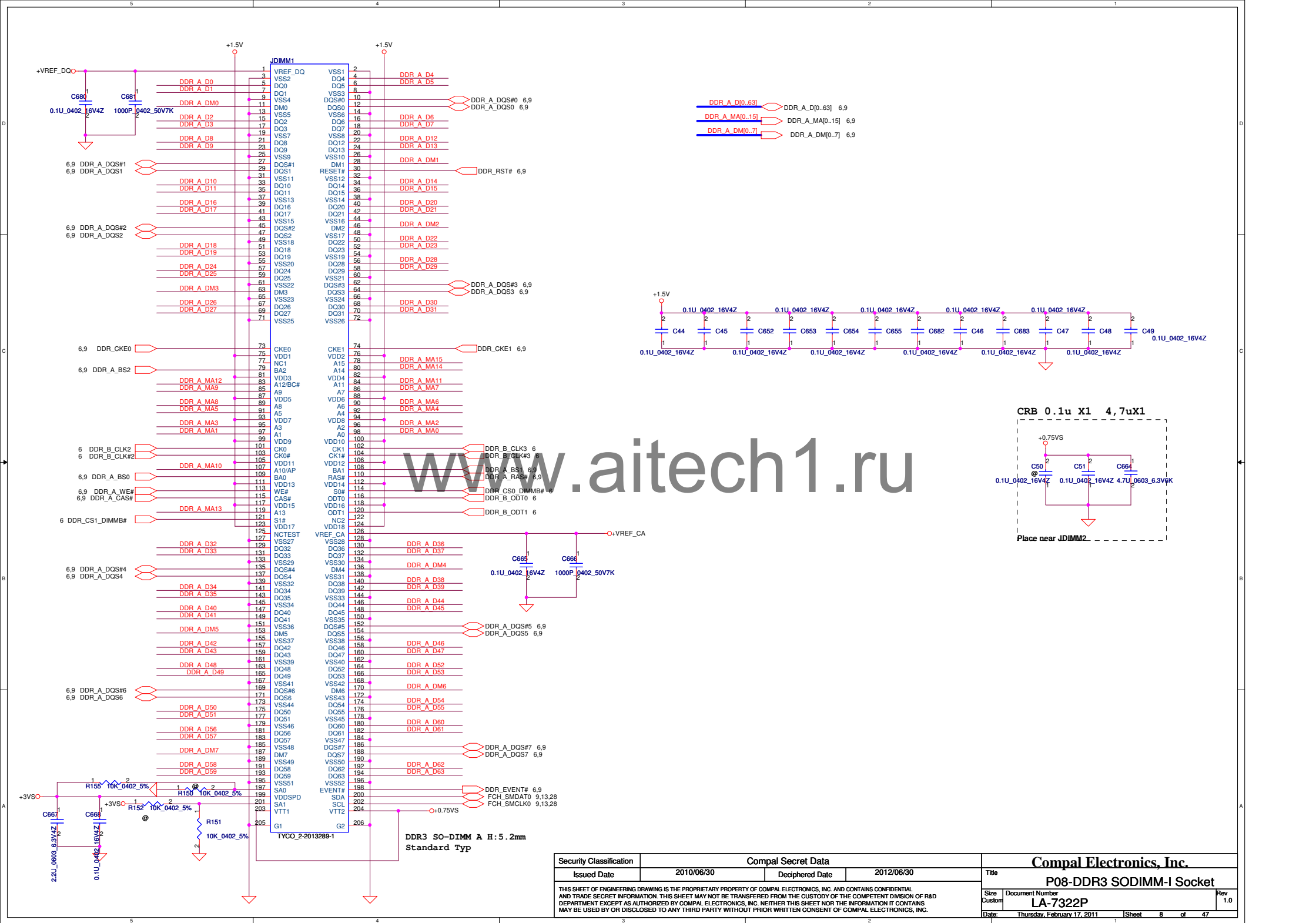
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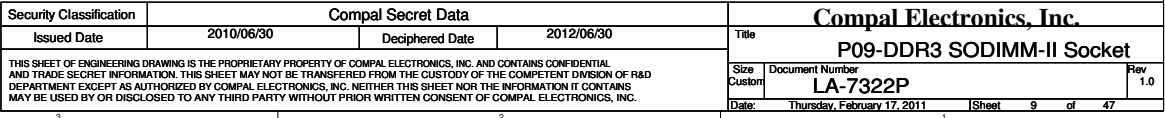
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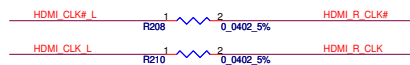
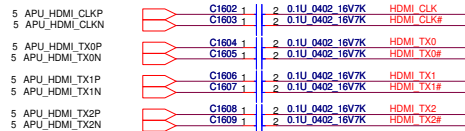
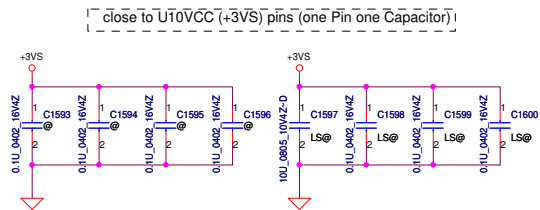




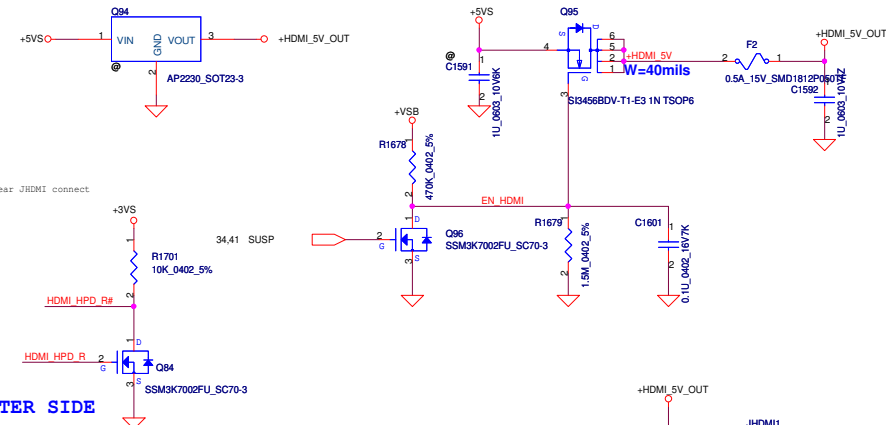
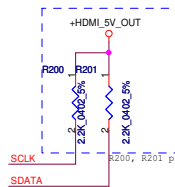
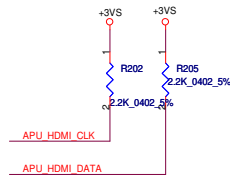
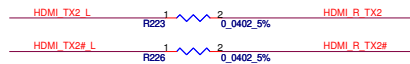
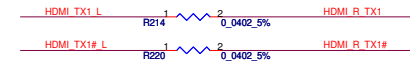
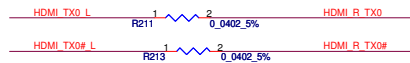
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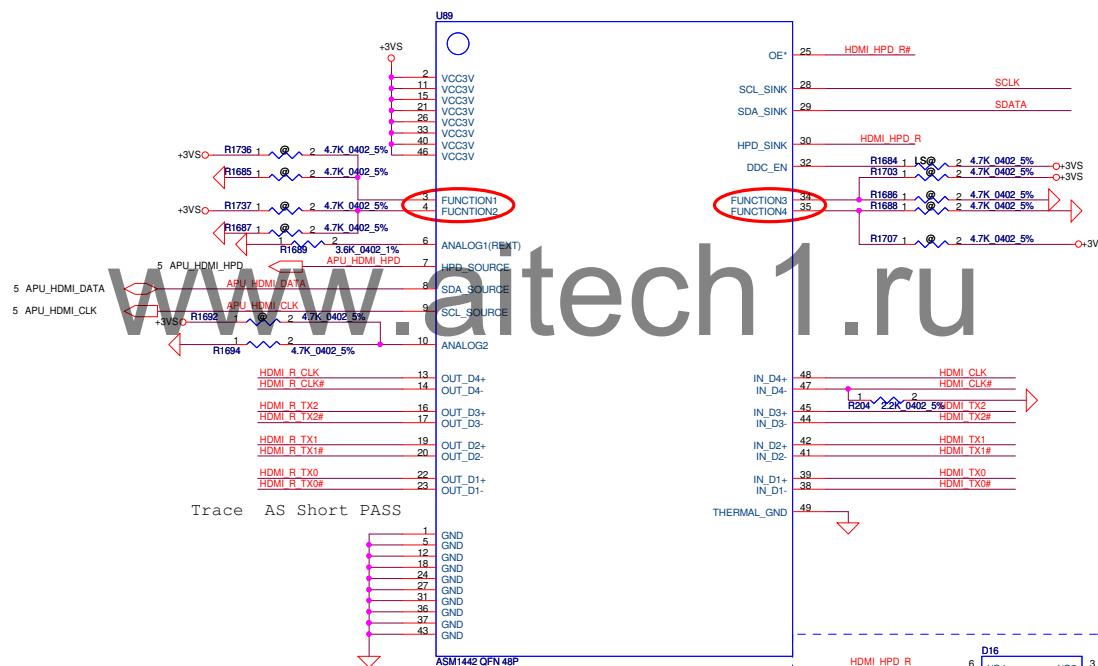




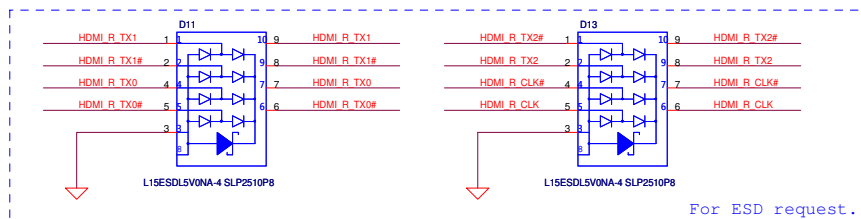
Swap signal for layout route.



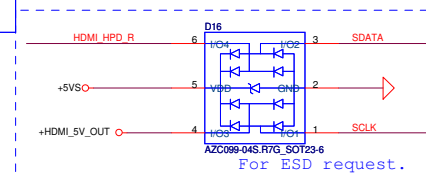
5V PULL UP IN CONNECTER SIDE



Trace AS Short PASS

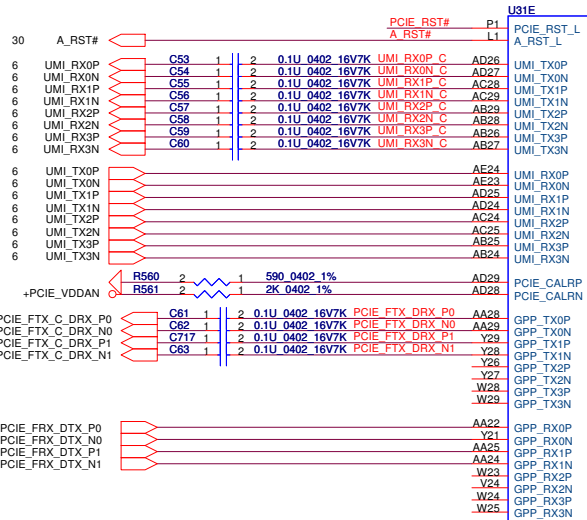


For ESD request.

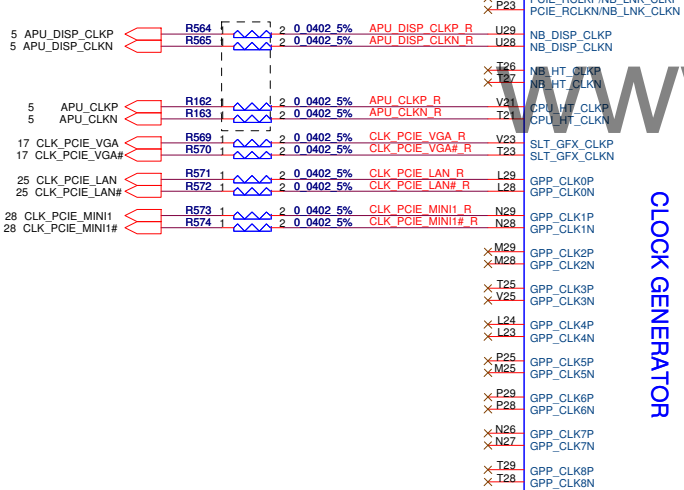


For ESD request.

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LAN
WLANLAN
WLAN

close to FCH within 1"



FCH : SA000046H60 (S IC 218-0792001 A12 HUDSON-M1 FCBGA 605P)
FCH : SA000046H70 (S IC 218-0792006 A13 HUDSON-M1 FCBGA 605P)

PCI CLKs

PCI EXPRESS I/F

PCI I/F

LPC

CPU

RTC

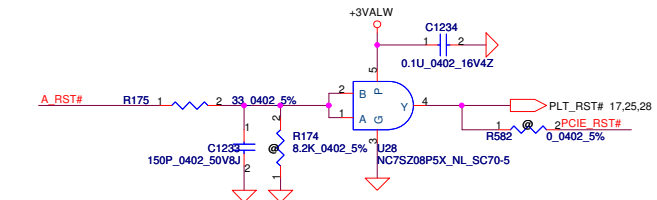
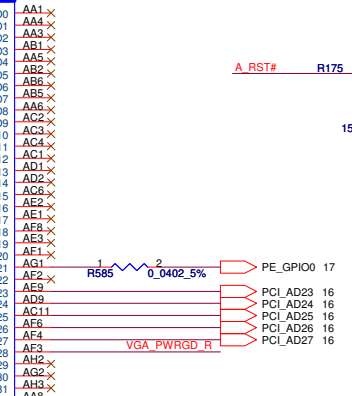
PCICLK0
PCICLK1/GPIO38
PCICLK2/GPIO37
PCICLK3/GPIO38
PCICLK4/14M_OSC/GPIO39

W2
W1
W3
W4
Y1

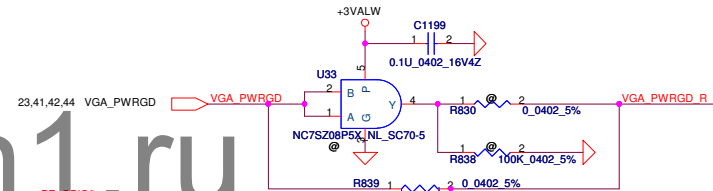
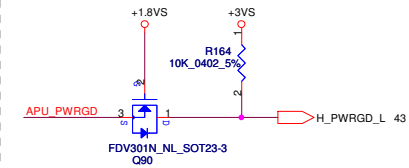
PCIRST_L

V2

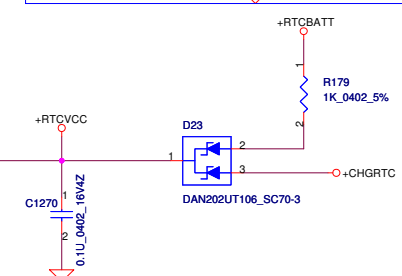
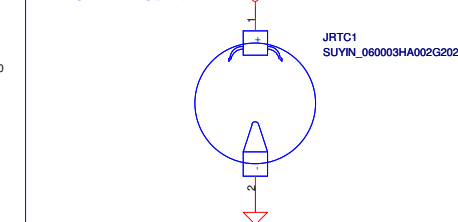
PAD T96
PAD T92



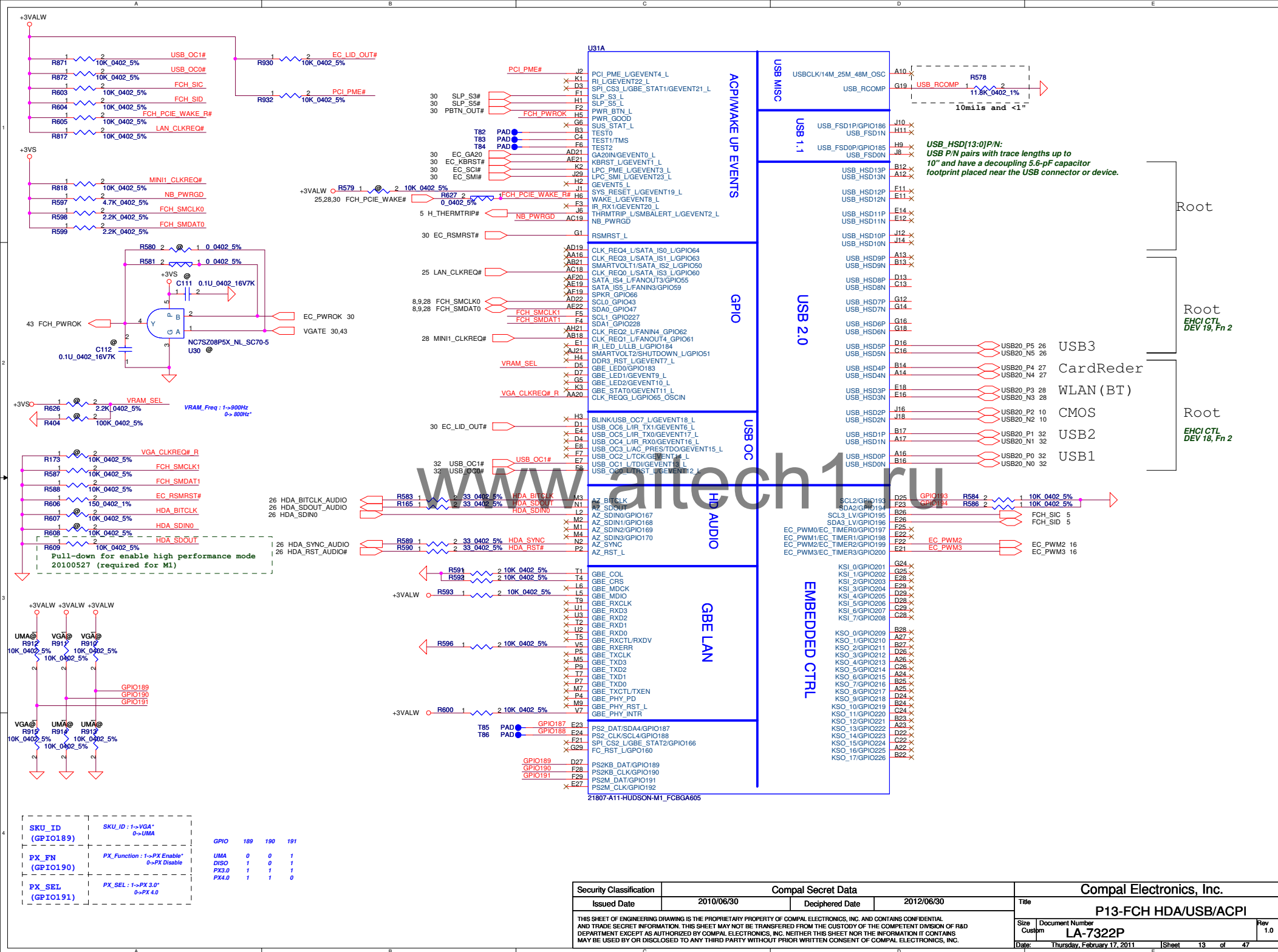
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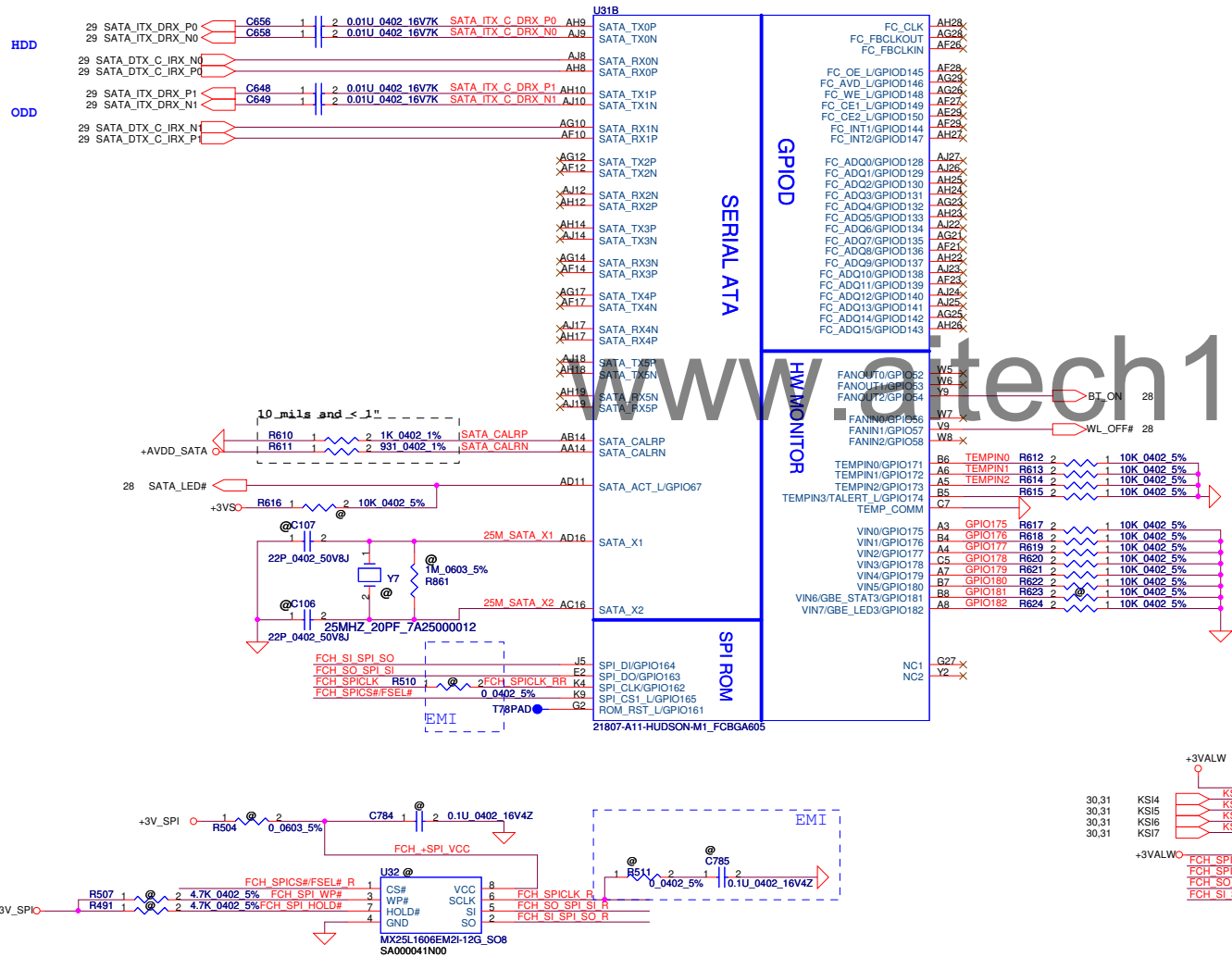


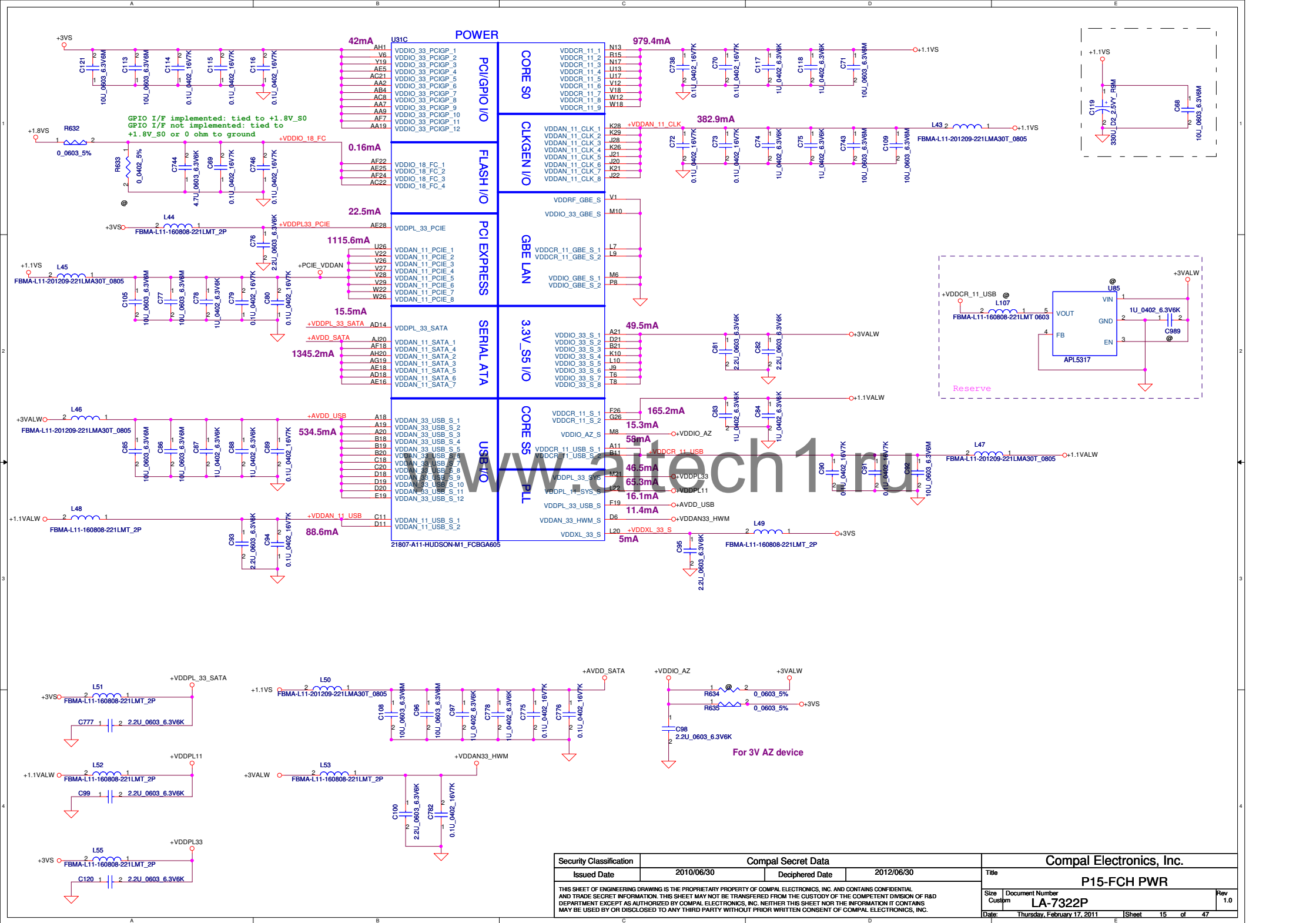
RTC BATT Conn.



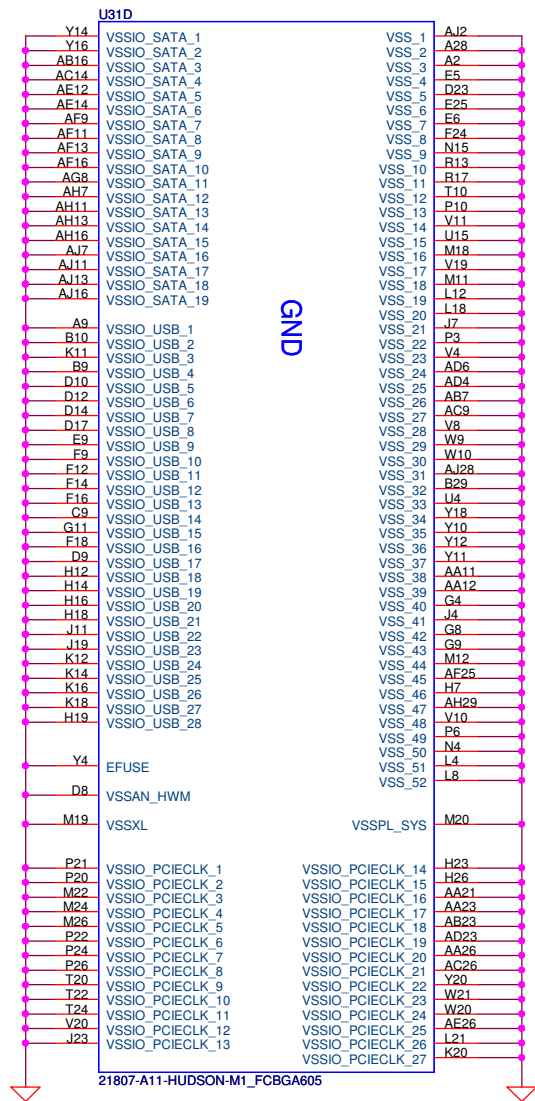
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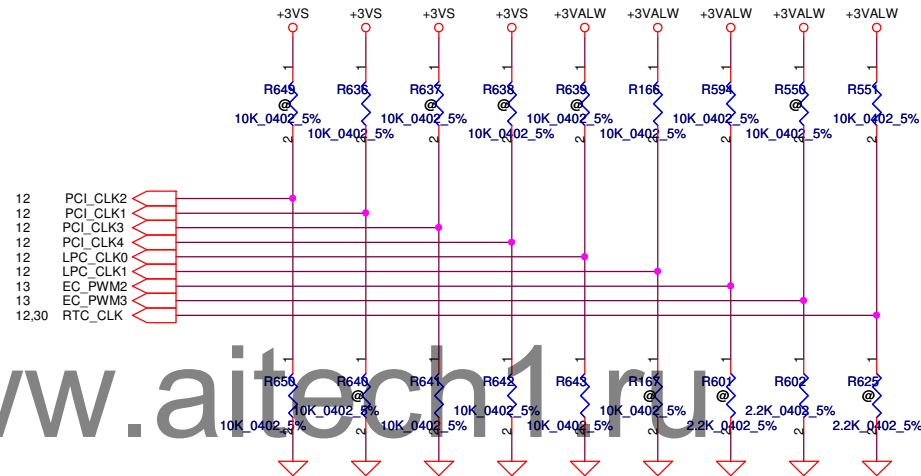
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REQUIRED STRAPS

Check Internal PU/PD

	PCI_CLK2	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	EC_PWM2 EC_PWM3
PULL HIGH	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	Internal EC ENABLE	Internal CLKGEN Mode DEFAULT	S5 PLUS MODE DISABLED DEFAULT	LPC ROM (H,L)
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK Mode DEFAULT	Internal EC DISABLE DEFAULT	External CLKGEN Mode	S5 PLUS MODE ENABLED	SPI ROM(L,H) .



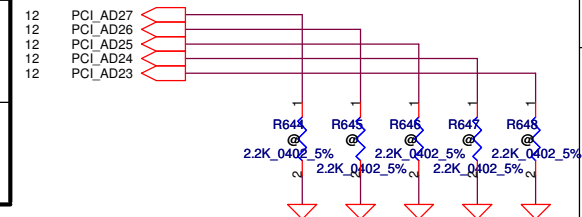
DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

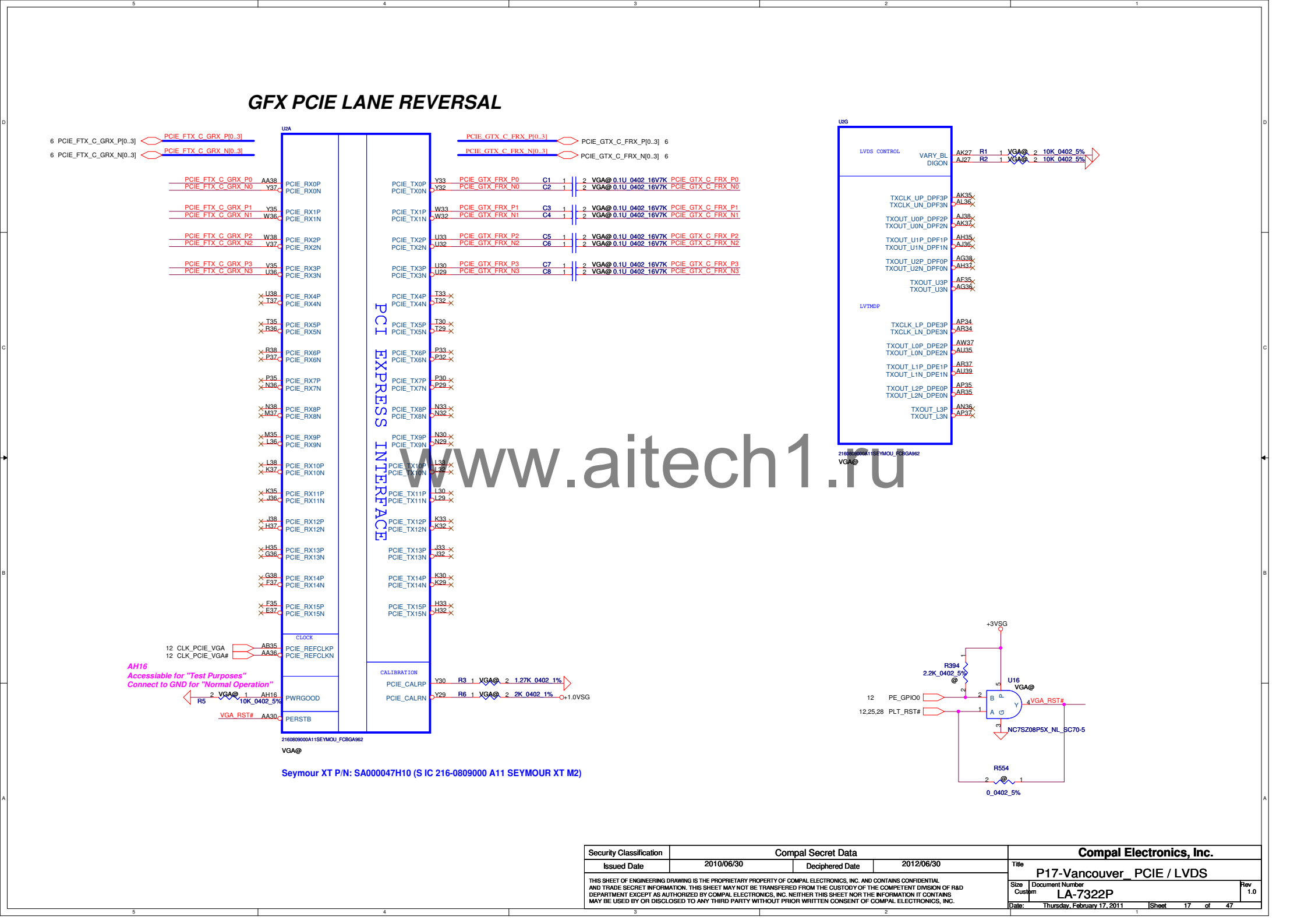
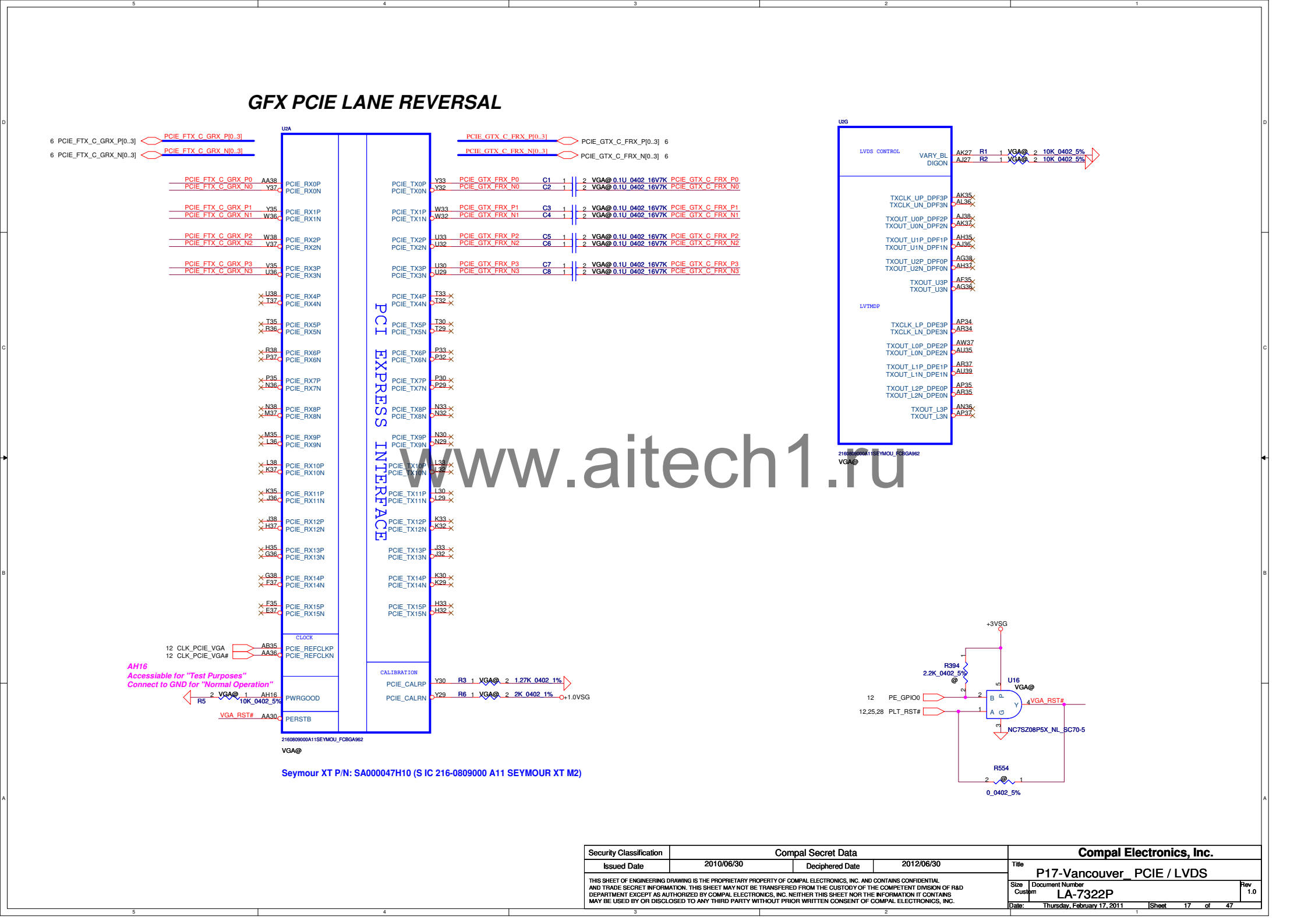
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH	USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function

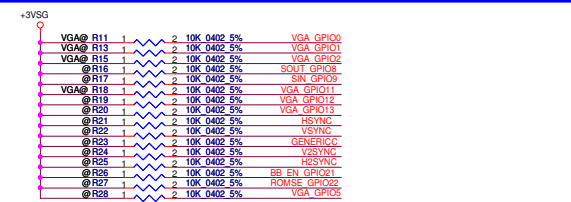
check default



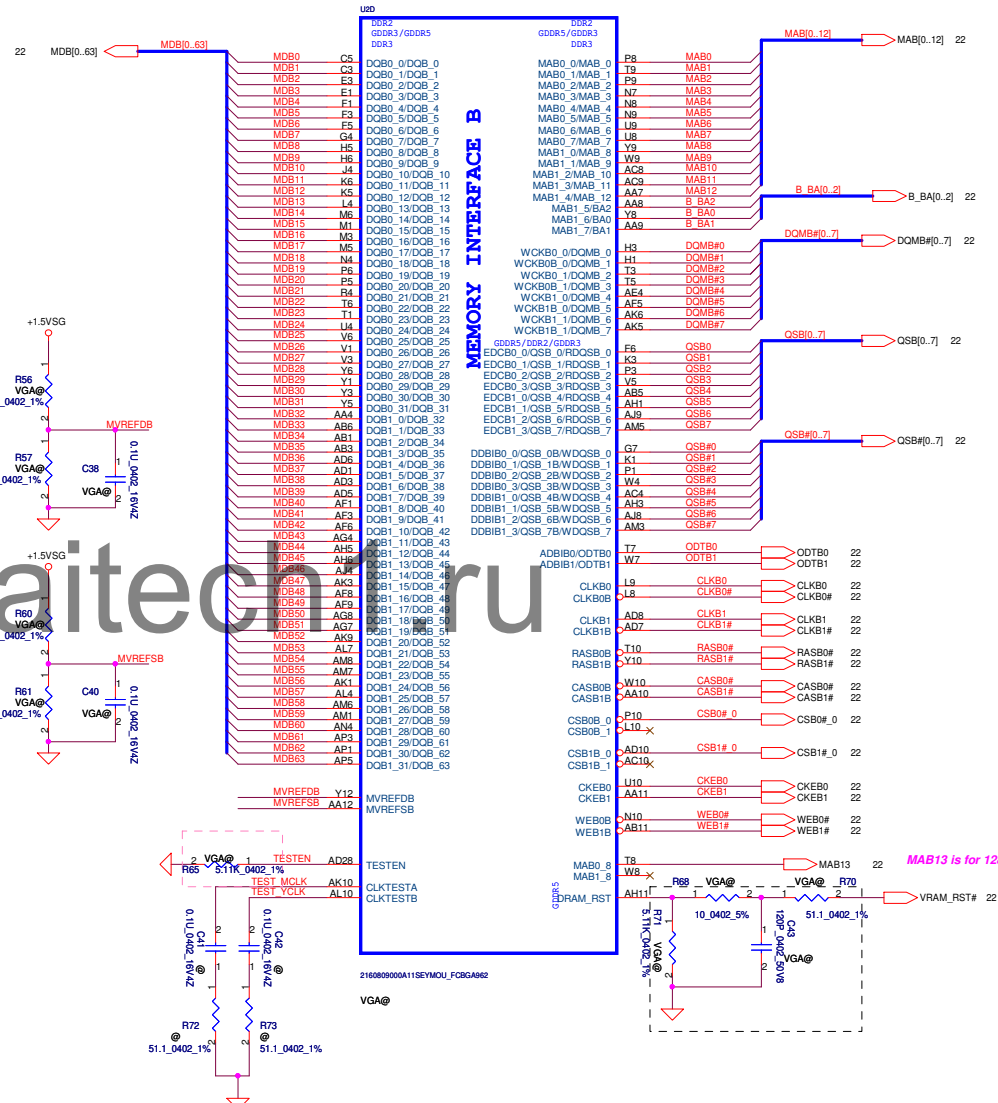
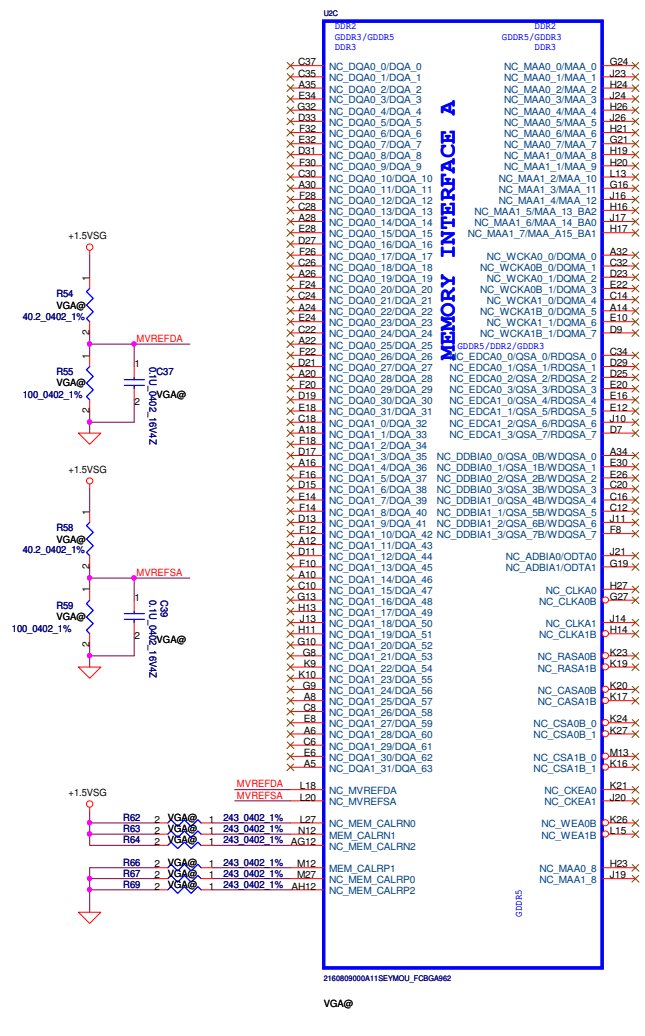
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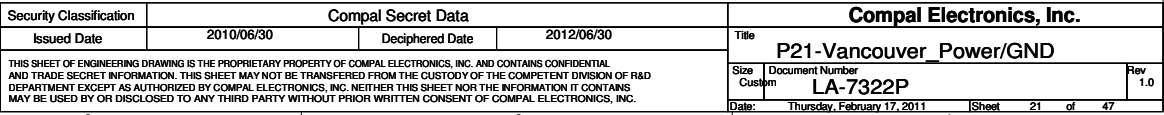
Strap Name		Pin Straps description <all internal PD>	Setting
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0): a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSVNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
BIF_GEN2_EN	GPIO2	0: Advertises the PCIe device as 2.5 GT/s capable at power-on 1: Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21 GENERICC GPIO5	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

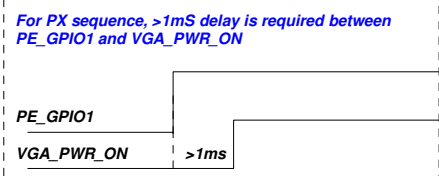


Robson, Seymour only support single channel memory (channel B only)

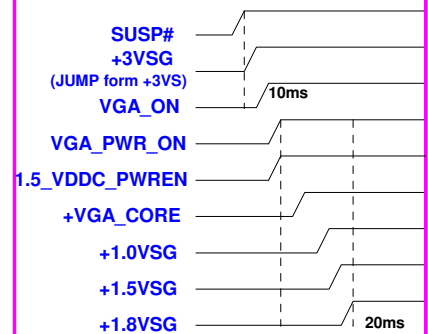


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				Custom	LA-7322P
				Date	Thursday, February 17, 2011
				Sheet	19 of 47



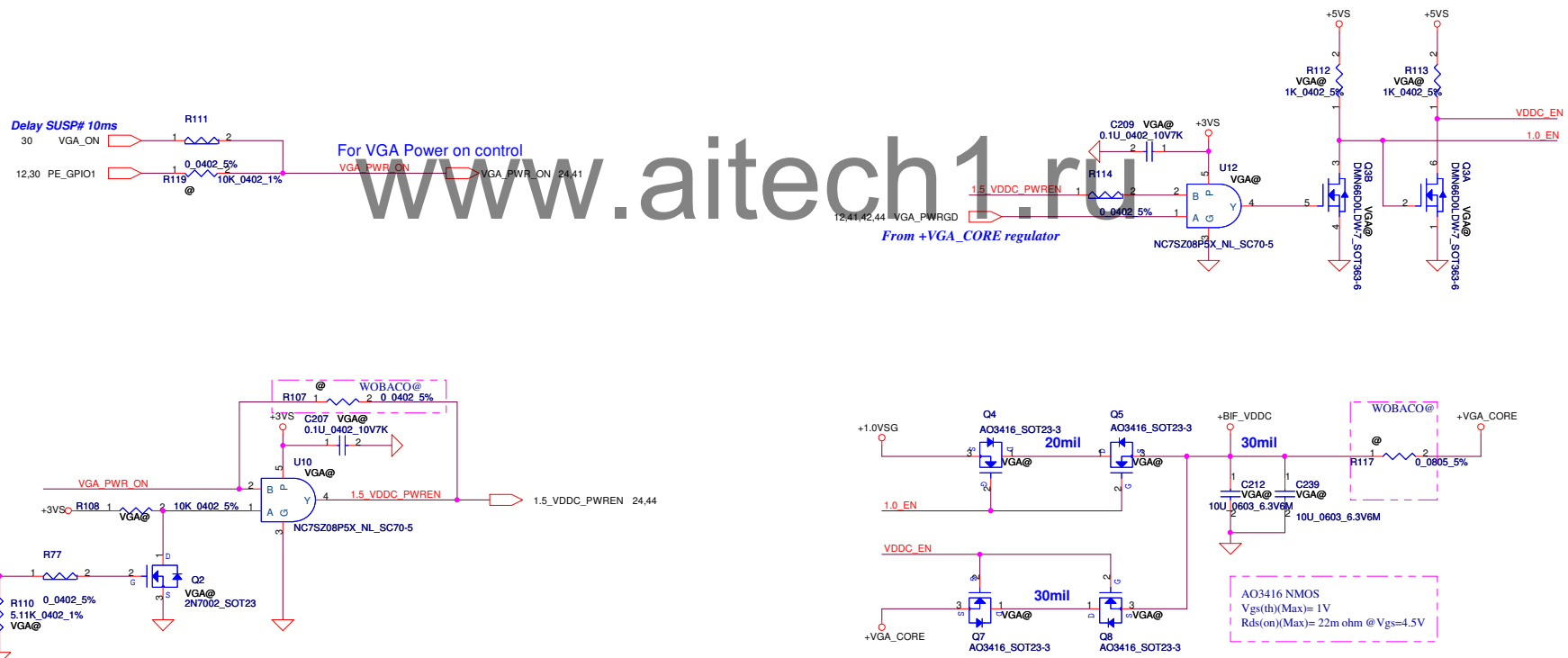


Power Sequence of Whistler and Seymour

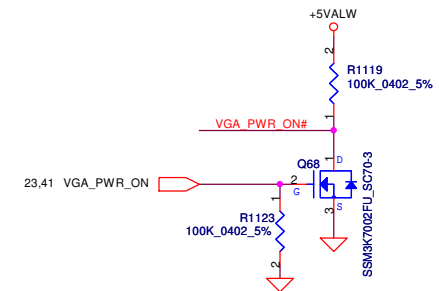
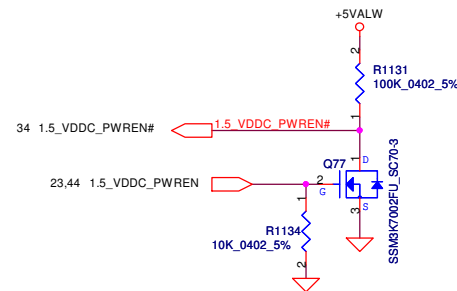
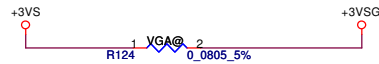


VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

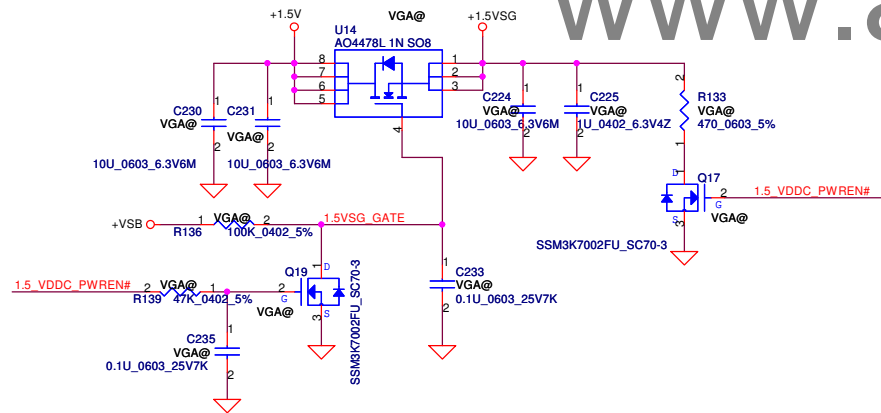
VGA Power Enable Signal Mapping table	
VGA_PWR_ON source signal	Seymour
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON#
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN#



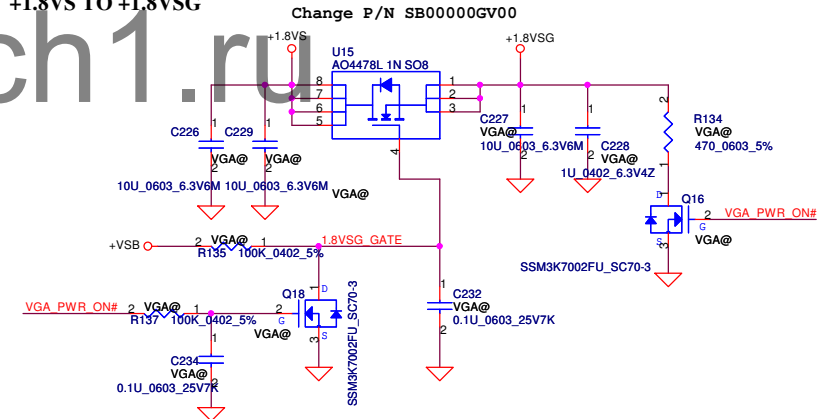
+3.3VS TO +3.3VSG



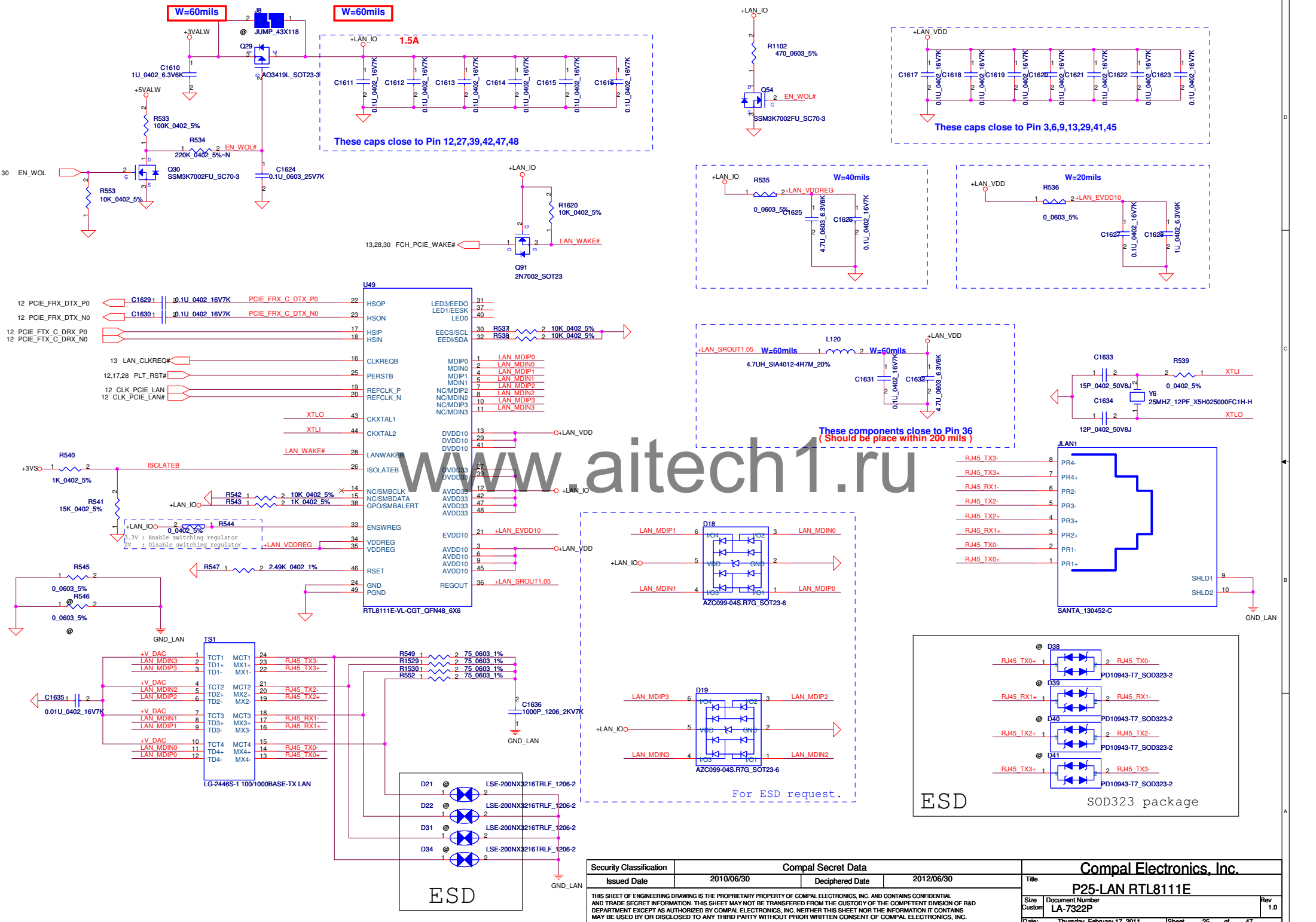
+1.5V TO +1.5VSG



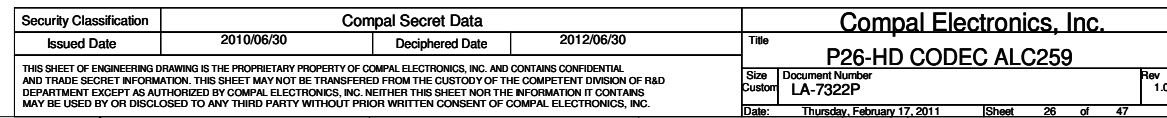
+1.8VS TO +1.8VSG



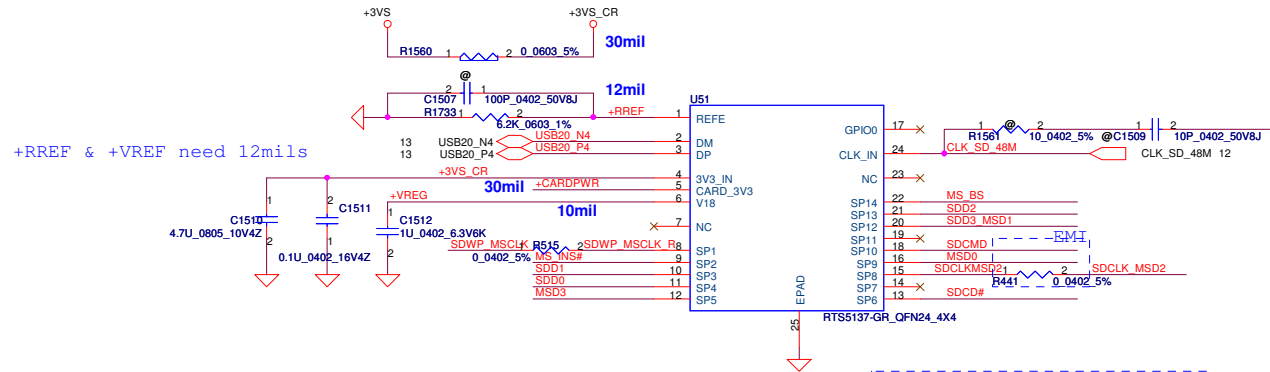
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Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title	
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Size		Document Number		Rev	
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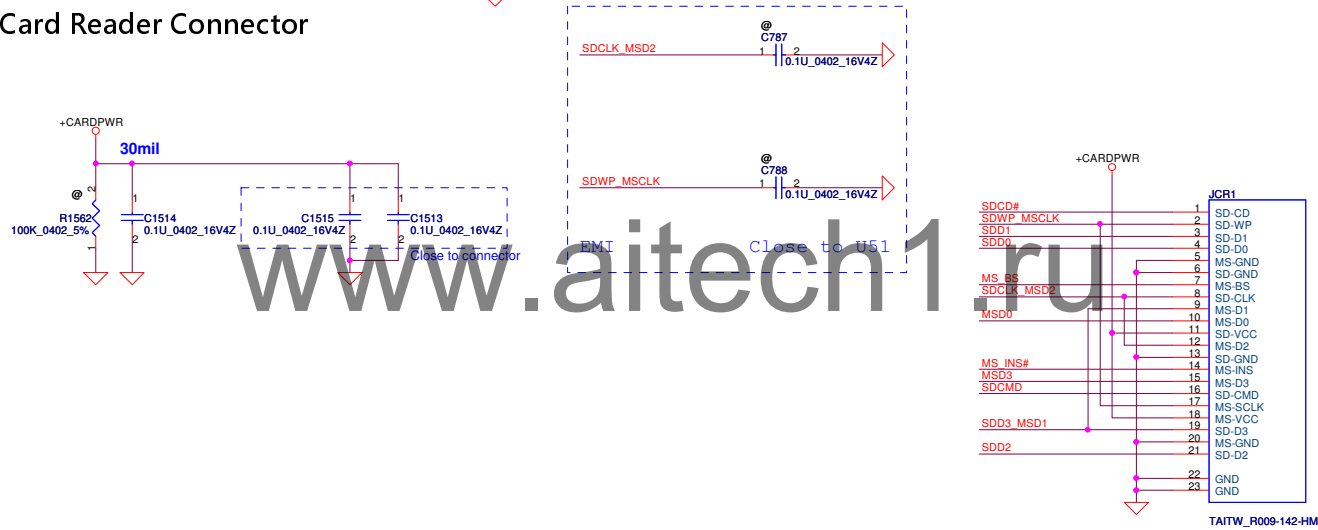
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Size	Custom	Document Number	LA-7322P	Rev	1.0
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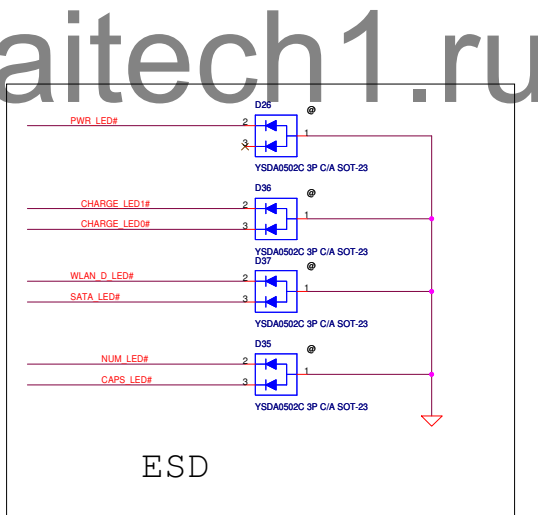
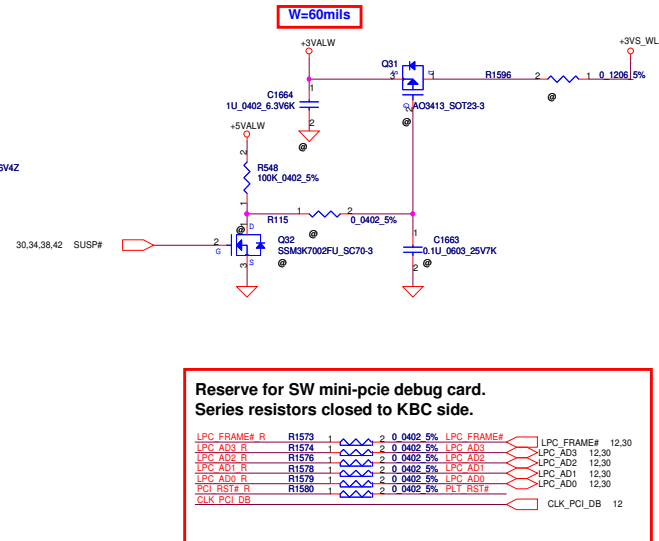
Card Reader RTS5137 (only SD/MMC/MS function)



Card Reader Connector

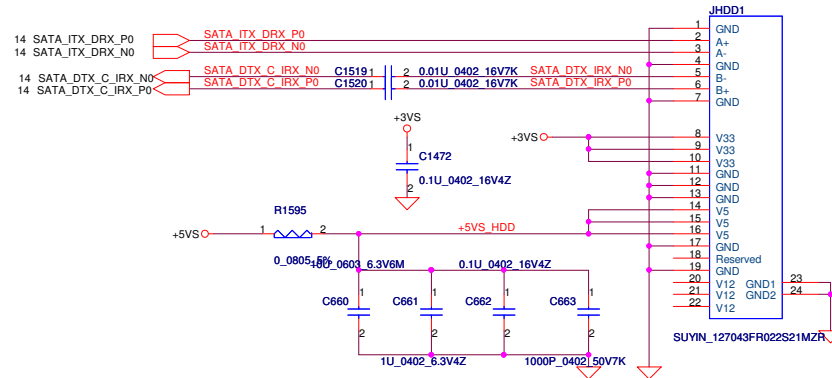


Mini-Express Card(WLAN/WiMAX)

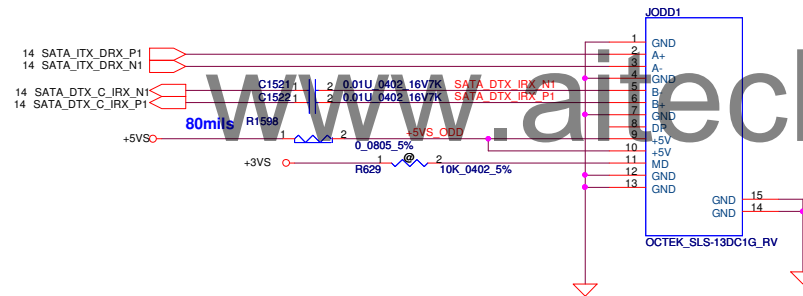


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						P28-Mini PCIE/LED				
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									LA-7322P	
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SATA HDD Conn.

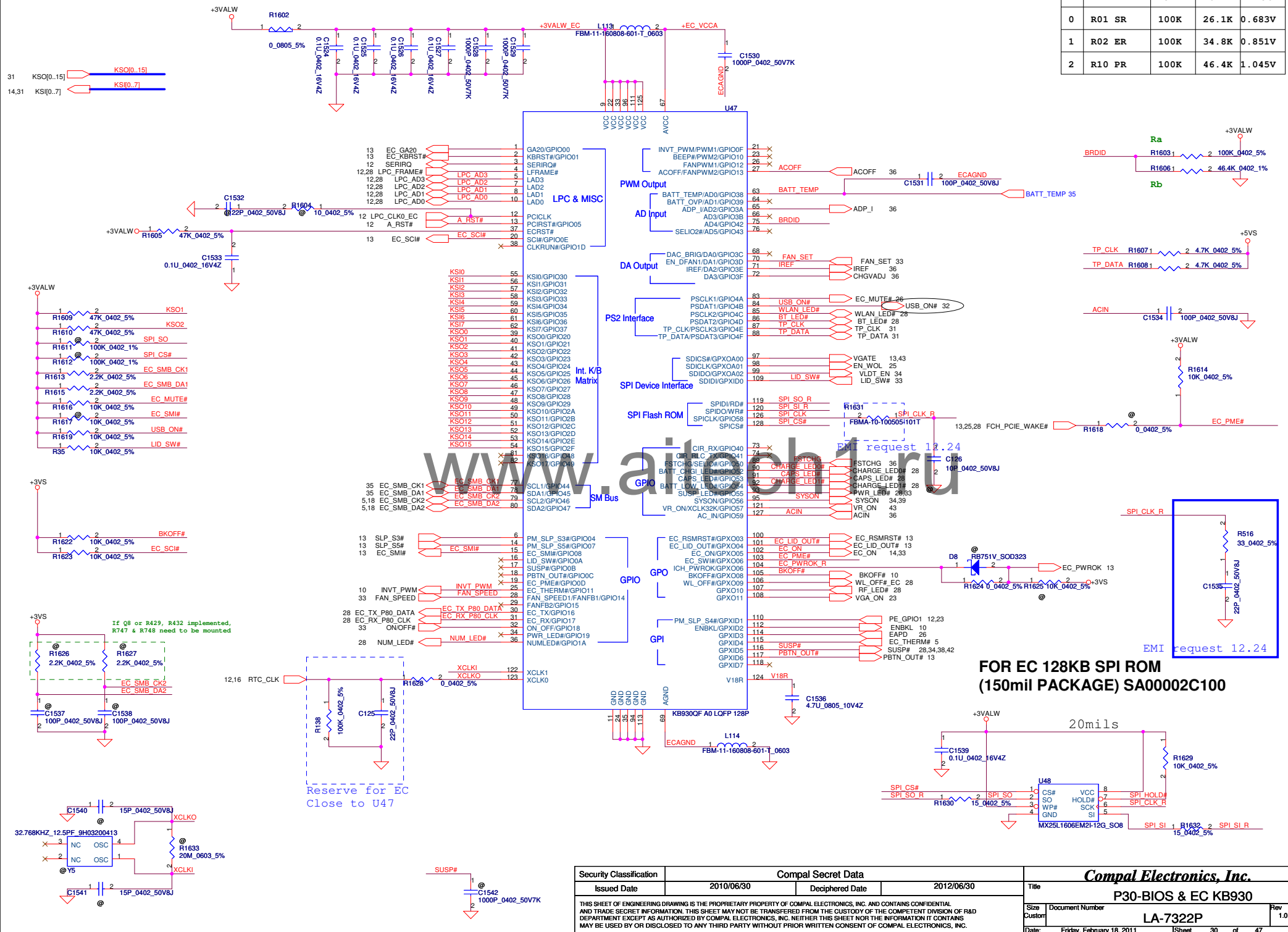


SATA ODD FFC Conn.



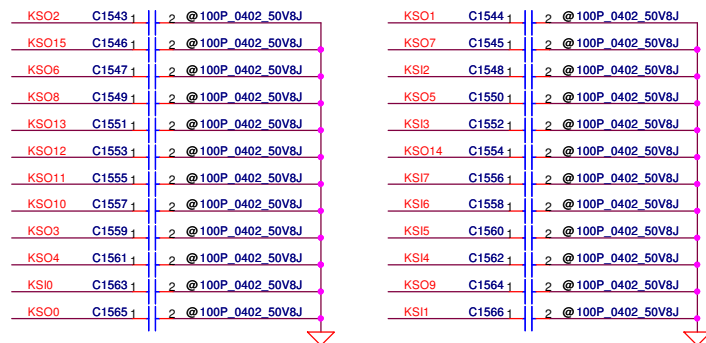
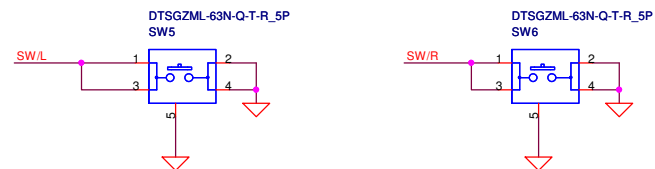
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ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	26.1K	0.683V
1	R02 ER	100K	34.8K	0.851V
2	R10 PR	100K	46.4K	1.045V

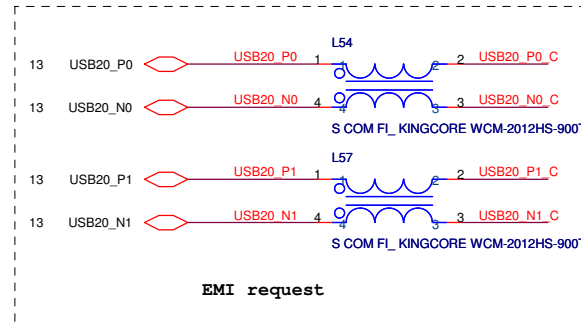


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										P30-BIOS & EC KB930							
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										Custom		LA-7322P		1.0			
										Date:		Friday, February 18, 2011		Sheet		30 of 47	

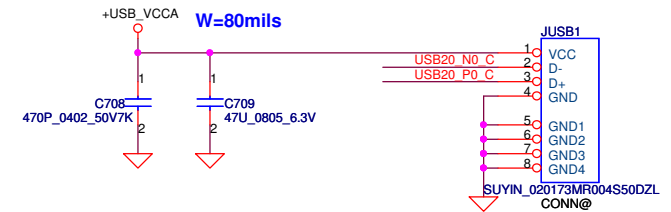
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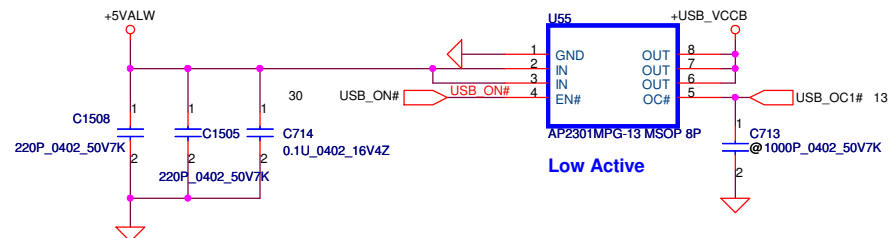
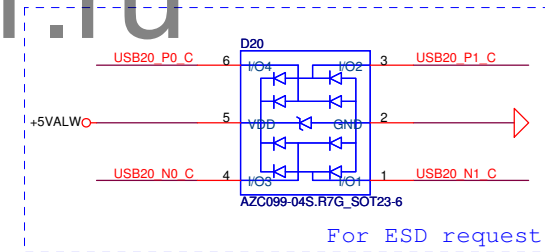
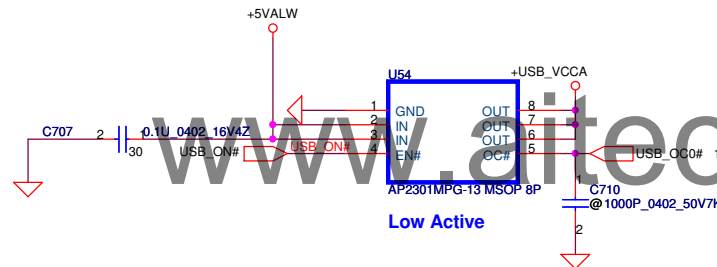
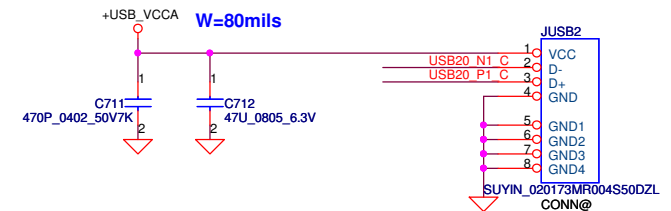
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Left USB Conn.

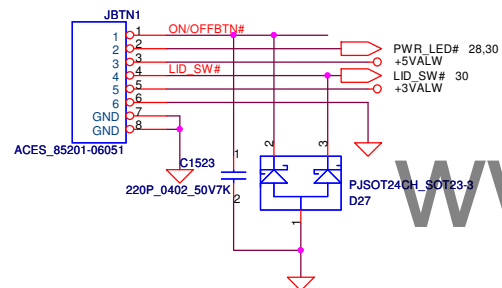
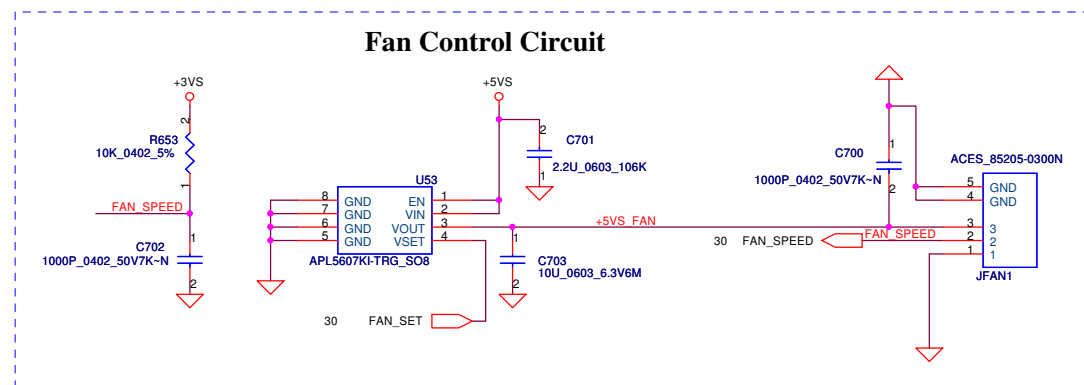
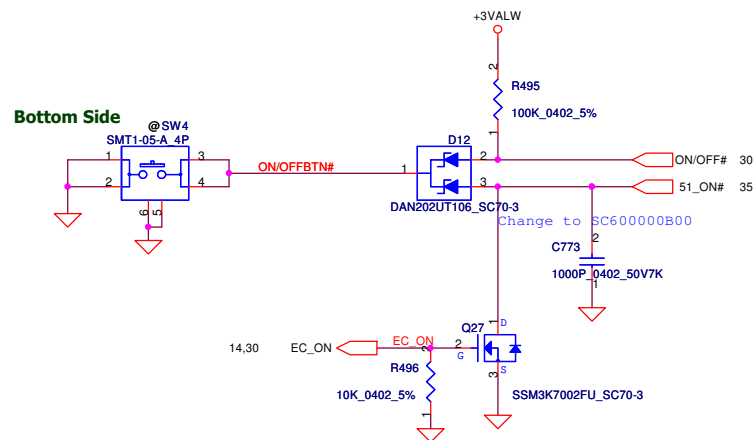


Left USB Conn.

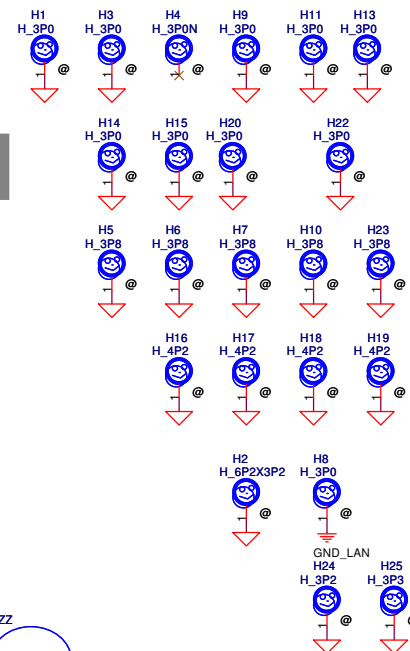


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ON/OFF switch **Power Button**



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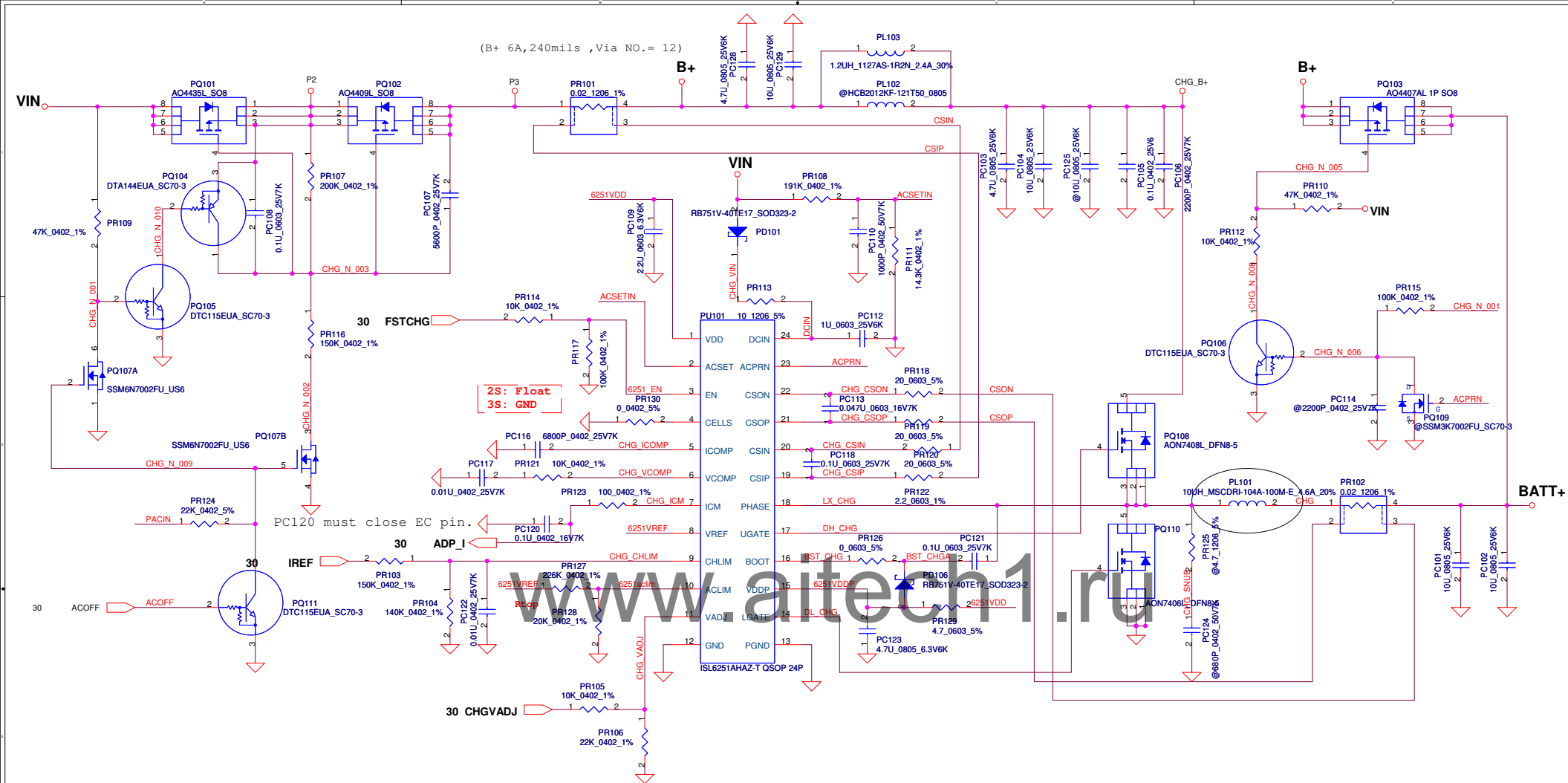


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Size Custom		Document Number		Rev	
		LA-7322P		1.0	
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Change P/N SB000000HZ00



(B+ 6A,240mils ,Via NO.= 12)



CP= 85%*Iada;

Iada=0~4.737A (90W); CP=4.03A; where Racdet=0.020ohm, where Rtop=12.4K
90W for Dis:Rtop:SD00000AJ80
Iada=0~3.421A (65W); CP=2.91A; where Racdet=0.020ohm, where Rtop=226K
65W for UMA:Rtop:SD034226380
Astro2010_01_15 need confirm P/N

CP mode

Vaclim=VREF*(Rbot//Rinternal/(Rtop//Rinternal+Rbot//Rinternal))
when 90W Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W Vaclim=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
Iinput=(1/Racdet)*((0.05*Vaclim/VREF+0.05))
when 90W, Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W, Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A

CC=0.25A-3A

IREF=1.016*Icharge

IREF=0.254V-3.048V

VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell CHGVADJ

4V 0V

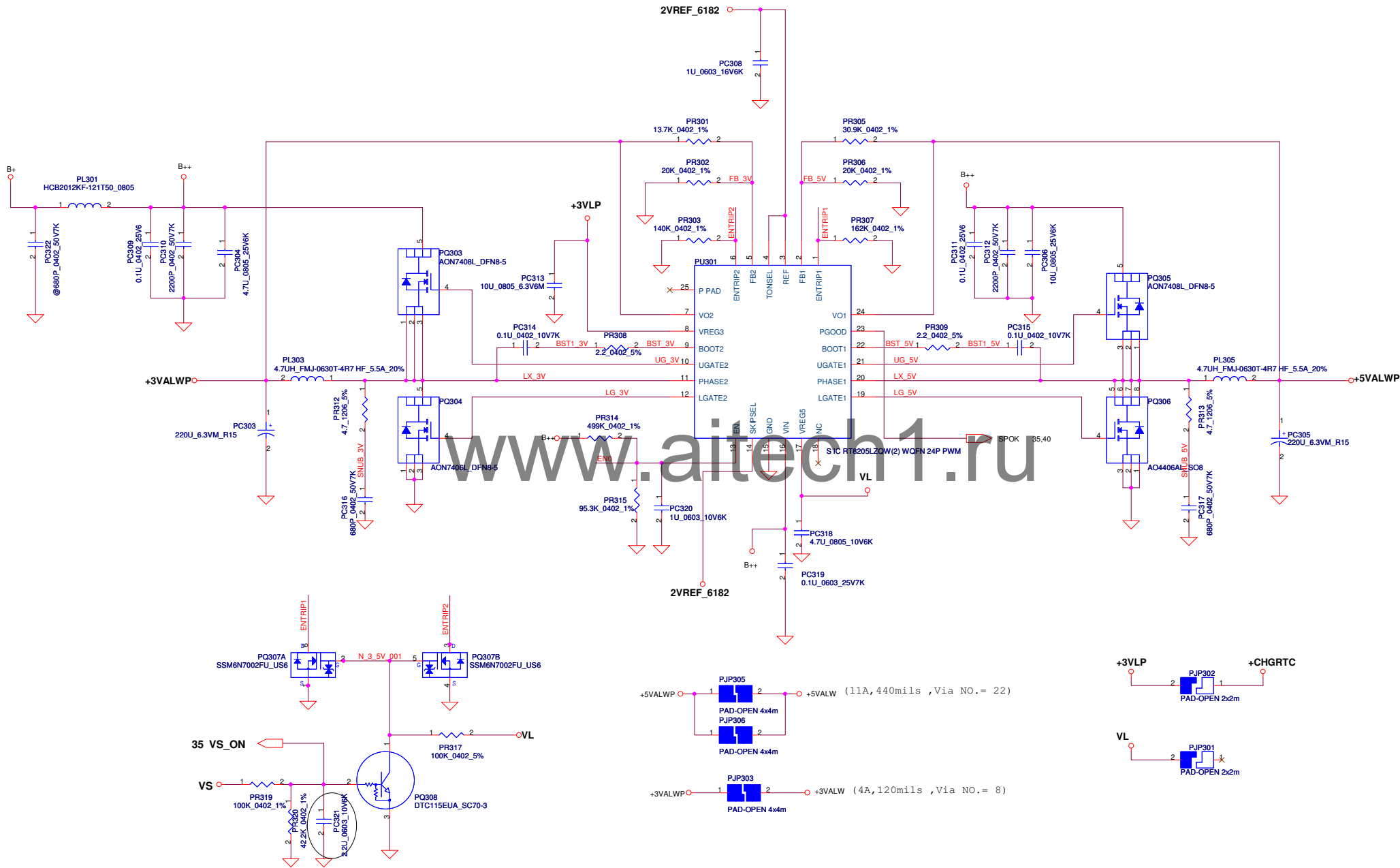
4.2V 1.882V

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Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1
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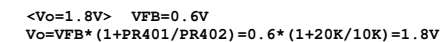


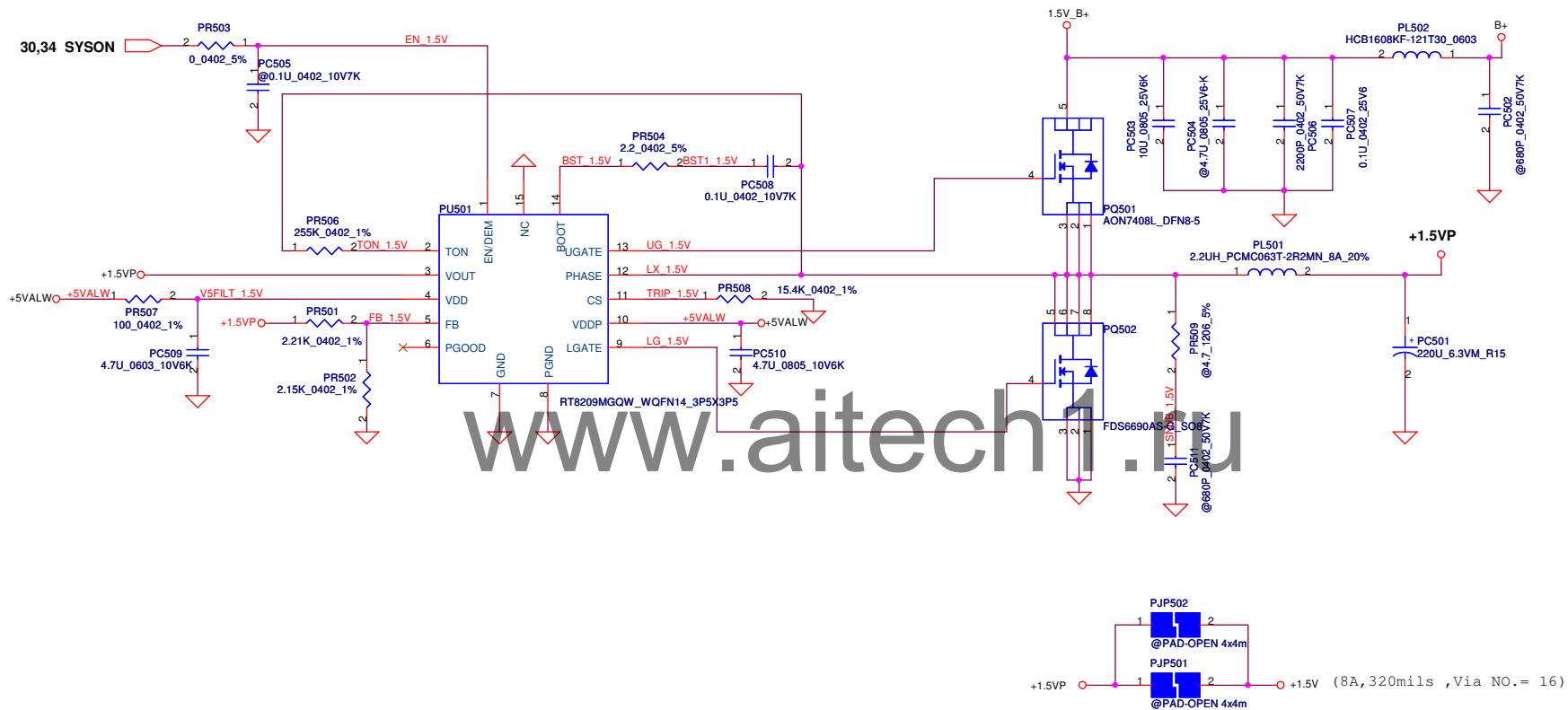
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				Sheet	37 of 44

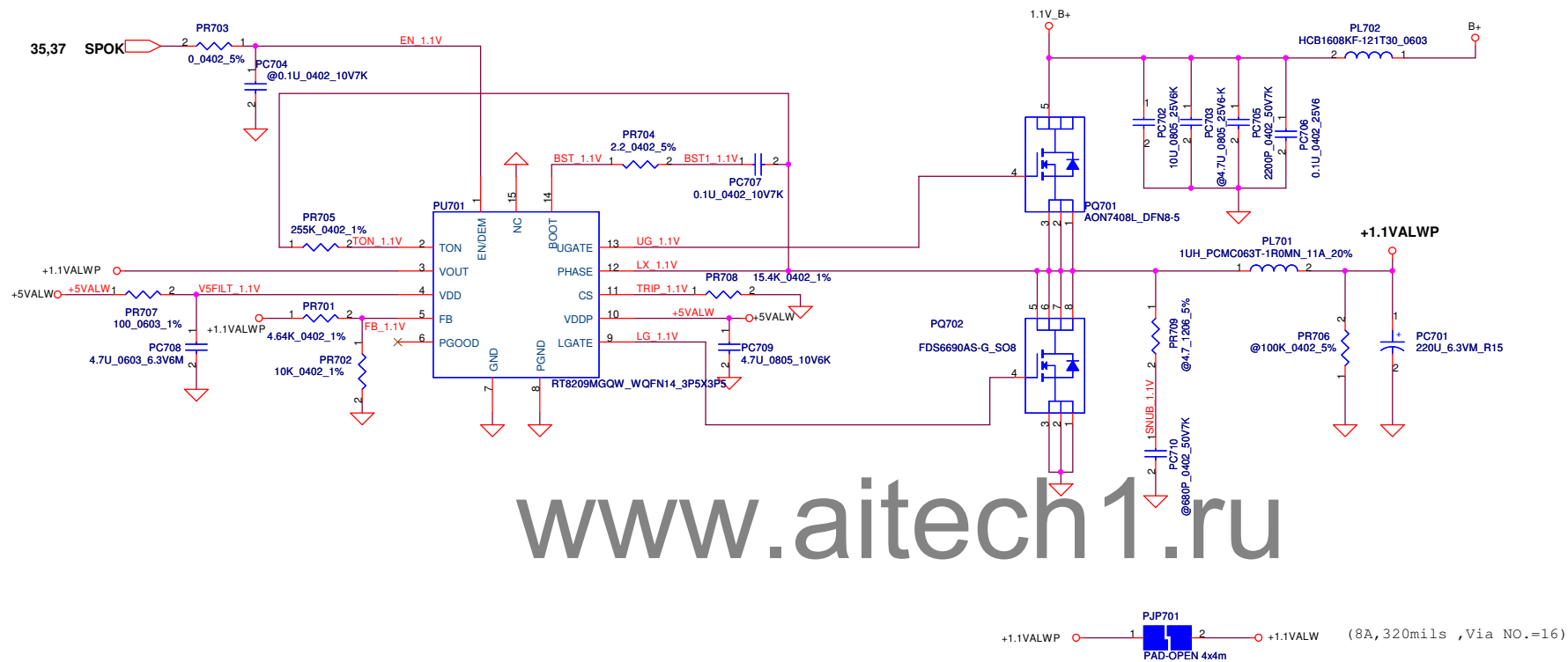
Compal Electronics, Inc.
3.3VALWP/5VALWP

Rev 0.1



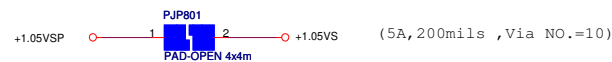
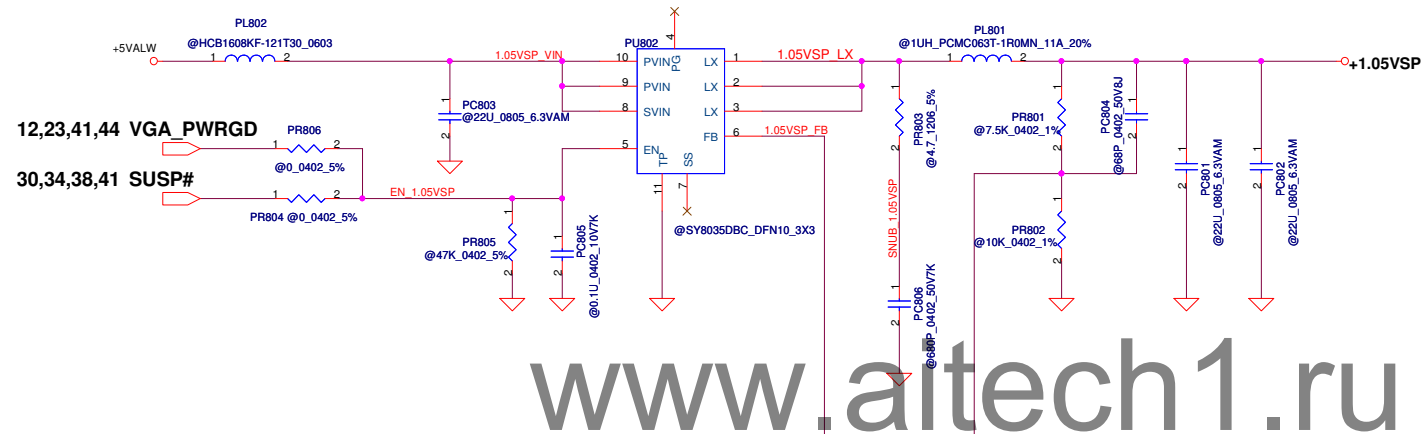


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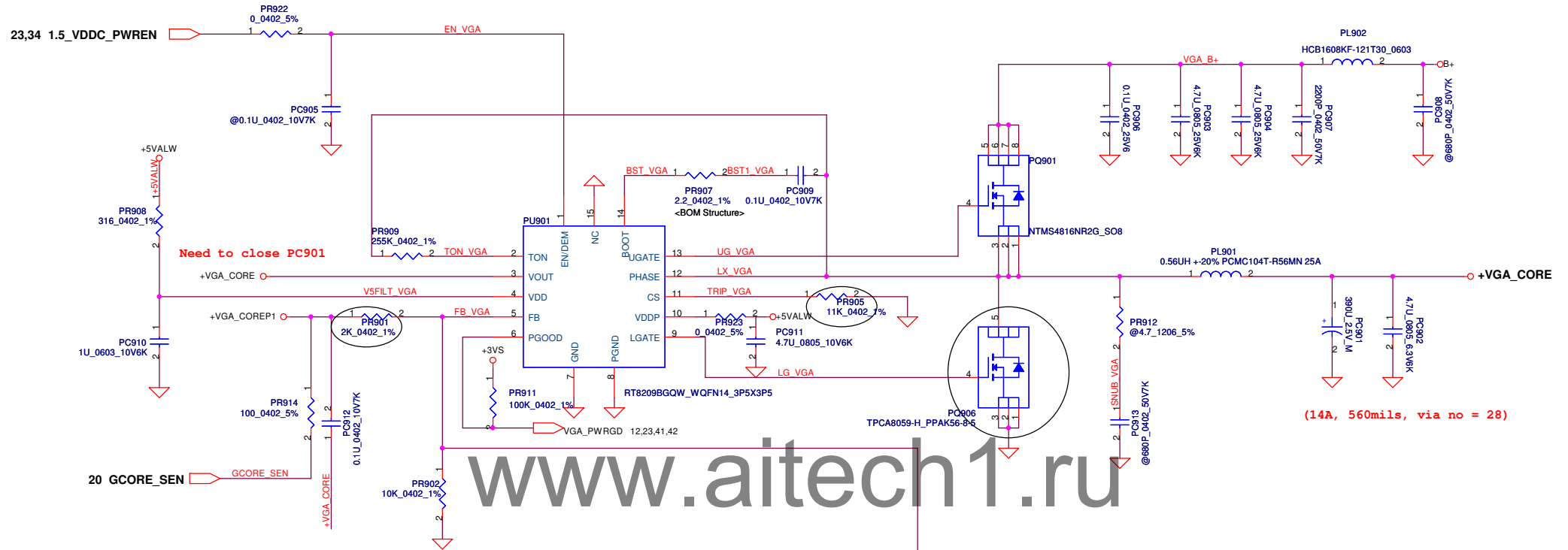


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				Date	Friday, February 18, 2011
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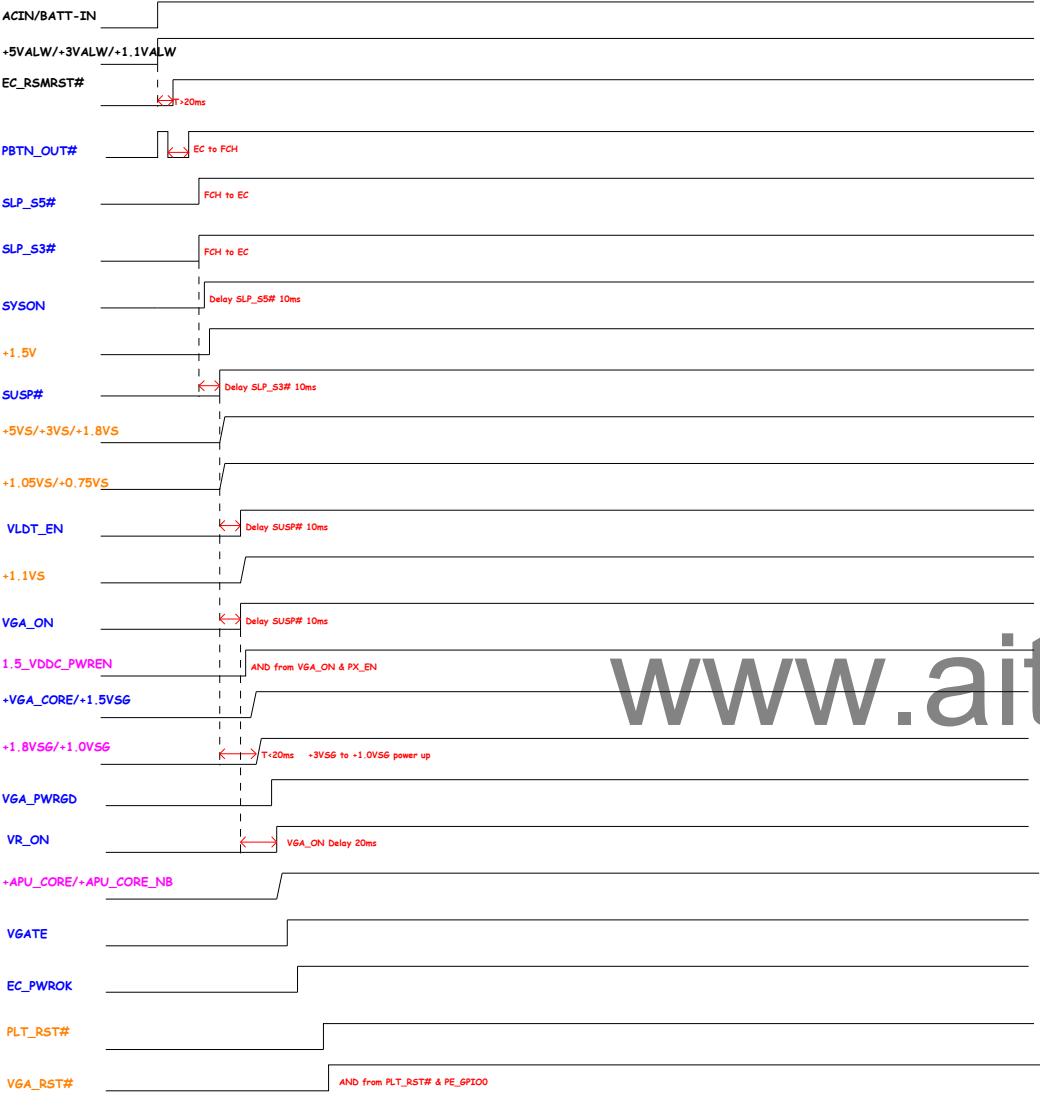
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GPU_VID1	GPU_VID0	+VGA_CORE
1	1	0.9V
0	1	1.05V
0	0	1.1V

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POWER SEQUENCE



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		TP FFC error	0.11	PG#31	Swap JTP1 pin define	12/15	ER
2		SW5 SW6 footprint error	0.11	PG#31	Update SW5 SW6 footprint	12/15	ER
3		FAN module connector pin define error	0.11	PG#33	Swap JFAN1 pin define	12/15	ER
4		DFB request to update footprint	0.11	PG#26 PG#33	Update JBTN1& JSPK1 footprint	12/15	ER
5		LID issue	0.11	PG#13	R930 change to pop	12/15	ER
6		LID issue	0.11	PG#30	LID_SW# added a pull up 10Kohm. (R35)	12/15	ER
7		Update Broad ID	0.11	PG#30	Change R1606 from 26.1Kohm to 34.8Kohm	12/15	ER
8		Double component	0.11	PG#34	Del Q54 & R1102	12/15	ER
9		Update PW schematic	0.11			12/16	ER
10		APU_THERMTRIP# of FCH SPEC	0.11	PG#05	R424 & Q79 change to unpop, R427 change to pop	12/17	ER
11		EC release note	0.11	PG#30	Add C125 & R138	12/17	ER
12		Crisis circuit	0.12	PG#14	Add UH6,R512,R513,R514	12/20	ER
13		DDR3 SPD	0.12	PG#08	Reserve R155 R152	12/21	ER
14		Update PW schematic	0.13			12/23	ER
15		Clear CMOS	0.13	PG#12	R865 change to CLRPI	12/23	ER
16		Procurement recommend	0.13		D4,Q97,Q29 change PN & footprint	12/23	ER
17		WLAN PW spec	0.13	PG#28	Reserve Q31 ,Q32 circuit	12/24	ER
18		EMI request	0.13	PG#26	R1544 change to L121	12/24	ER
19		EMI request	0.13	PG#30	R1631 change to FBMA-10-100505-101T	12/24	ER
20		EMI request	0.13	PG#30	R516 change to 33ohm, C1535 change to 22P	12/24	ER
21		LAN power	0.13	PG#25	Add R553 & J8	12/27	ER
22		EMI request	0.13	PG#25	R549,R552,R1529,R1530 change to 0603	12/27	ER
23		Update PW schematic	0.13			12/27	ER
24		Crystal EA	0.2	PG#18	C35,C36 change to 18P from 20P	12/29	ER
25		Crystal EA	0.2	PG#25	C1634 change to 10P from 27P C1633 change to 12P from 27P	12/29	ER
26		Crystal EA	0.2	PG#12	C66 change to 8.2P from 22P C67 change to 10P from 22P	12/29	ER
27		PE_GPIO1 pull down	0.2	PG#12	Add R109 for PE_GPIO1	12/29	ER

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